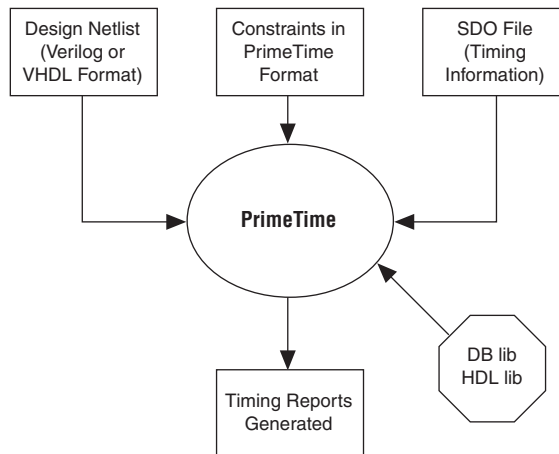


Introduction

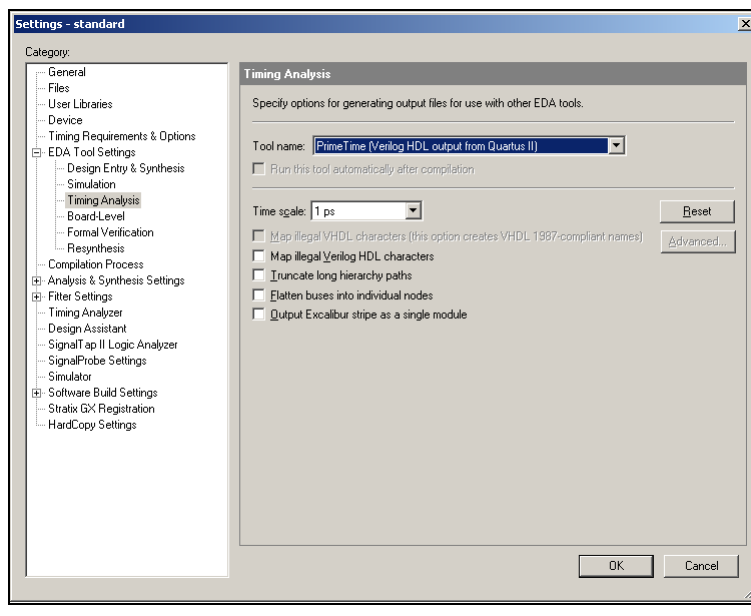
Prime Time is an industry standard sign-off tool, used to perform static timing analysis on most ASIC designs. The Quartus® II software provides a path to enable users to run Prime Time on their Quartus designs, exporting netlist, constraints specified in Quartus format, and libraries to the Prime Time environment. Figure 5–1 shows the Prime Time flow diagram.

Figure 5–1. Prime Time Flow Diagram



Quartus II Settings to Generate Prime Time Files

To set the Quartus II software to generate Prime Time files, choose **Settings** (Assignments menu). Choose **EDA Tool Settings > Timing Analysis** in the **Category** dialog box to display the **Timing Analysis** window. In the **Timing Analysis** window, click on the **Tool name** pull down menu and select **PrimeTime (Verilog HDL output from Quartus II)** or **Prime Time (VHDL output from Quartus II)**, as shown in Figure 5–2. This setting enables the Quartus II software to produce three files for the Prime Time tool, which are then written into the **timing/primetime** directory of the current project.

Figure 5–2. Setting the Quartus II Software to Generate Prime Time Files

Files Generated for the Prime Time Environment

This section describes the three files that the Quartus II software creates for the Prime Time tool.

- `<project_name>.vo` or `<project_name>.vho` files

This is the netlist file written in either Verilog (`.vo`) or VHDL (`.vho`) format, depending on the format selected in the EDA settings. This file contains the flat netlist representing the entire design.

- `<project_name>_v.sdo` or `<project_name>_vhd.sdo` files

These files contain the timing information for each timing arc in the design. Like the netlist files, these files are written in either Verilog (`_v`) or VHDL (`_vhd`) format, depending on the selection made in the EDA settings. This file corresponds to the worst-case delay values of the timing arcs if regular timing analysis is performed in Quartus.

If you want to use the best-case delay values for Prime Time analysis, you must perform a Minimum Timing Analysis in the Quartus II software. This is a two-step process, as follows:

1. Select **Start > Start Minimum Timing Analysis** (Processing menu).
2. Select **Start > Start EDA Netlist Writer** (Processing menu).

This will create a `<project_name>_v_min.sdo` or `<project_name>_vhd_min.sdo` file, which contains the best-case delay values for each timing arch.



It is up to you to point to either best-case or worst-case delay values during the Prime Time processing by specifying the appropriate file name in the Tool Command Language (Tcl) script file described below.

■ `<project_name>_pt_v.tcl` or `<project_name>_pt_vhd.tcl` files

These files contain the search path to, and the names of, the Prime Time database library files provided by Altera. A file referred to in this Tcl file (**device_all_pt.v** or **device_all_pt.vhd**) contains the Verilog/VHDL description of each library cell. The search path and link path are defined at the beginning of the Tcl file. The search path must be modified, depending on where these libraries are stored. The link path contains the names of all database files, and it does not need to be modified.

Here is an example of the search path and link path defined in the Tcl file:

```
set quartus_root ". /apps1/altera/quartus/II-3.0"

set search_path [list . $quartus_root
/appsl/altera/quartus/II3.0/eda/synopsys/primetime/lib ]

set link_path [list * stratix_asynch_io_lib.db
stratix_io_register_lib.db stratix_lvds_receiver_lib.db
stratix_asynch_lcell_lib.db stratix_lvds_transmitter_lib.db
stratix_core_mem_lib.db stratix_lcell_register_lib.db
stratix_mac_out_internal_lib.db stratix_mac_mult_internal_lib.db
stratix_mac_register_lib.db stratix_memory_register_lib.db
stratix_pll_lib.db alt_vt1.db]

read_verilog stratix_all_pt.v
```

This Tcl file also contains equivalent constraints in Prime Time format, converted automatically by the Quartus II software from constraints in Quartus II format. Additional Prime Time commands can be placed in the Tcl file to report on, or analyze, timing paths. This Tcl file also has a command to read the SDO file generated by the Quartus II software. Depending on which SDO file is desired, either with best-case or worst-case delays, the appropriate SDO file name should be specified.

Sample of Constraints Specified in Prime Time Format

The Prime Time constraints shown in [Table 5-1](#) are automatically generated by the Quartus II software. The `set_input_delay -max` command is equivalent to the t_{SU} constraint in the Quartus II software. Since `input_delay` in Prime Time is defined as the data delay from clock edge to the input pin, and t_{SU} in the Quartus II software is the data delay from the input pin to clock edge, t_{SU} is subtracted from the clock period to calculate the `set_input_delay`. [Table 5-1](#) shows the automatically-generated Prime Time constraints and their Quartus II software equivalents.

Table 5-1. Equivalent Quartus II & Prime Time Constraints

Prime Time Constraint	Quartus II Equivalent
<code>create_clock -period 10.000 -waveform {0 5.000} [get_ports clk] \-name clk</code>	Clock defined on input pin, clock of 10 ns period 50% duty cycle
<code>set_input_delay -max -add_delay 9.000 -clock [get_clocks clk] \ [get_ports din]</code>	t_{SU} of 1 ns on input pin, din
<code>set_input_delay -min -add_delay 1.000 -clock [get_clocks clk] \ [get_ports din]</code>	t_H of 1 ns on input pin, din
<code>set_output_delay -max -add_delay 7.000 -clock [get_clocks clk] \ [get_ports out]</code>	t_{CO} of 3 ns on output pin, out

Prime Time Timing Reports

This section describes the timing reports that the Prime Time tool generates, and the Tcl script commands that control each report's contents.

- `report_timing -nworst 100 > file.timing`

This command, which can be inserted at the end of the Tcl file to report timing paths in Prime Time, will generate a list of the 100 worst paths, and place this data into a file called `file.timing`.

Timing paths in Prime Time are listed in the order of most-negative-slack to most-positive-slack. Failing paths are not reported under each constraint's category, as they are in the Quartus II software. Timing setup (t_{SU}) and timing hold (t_H) times are not listed separately. In Prime Time, there is a start and end point given with each path to identify, for example, if it is a register-to-register or input-to-register type of path. If you only use the `report_timing` part of the command without adding a `-delay` option, only the setup-time-related timing paths are reported.

■ `report_timing -delay min`

This command is used to create a minimum timing report or a list of hold-time-related violations. It is up to you to define what type of SDO file is being used. Both minimum delay and maximum delay SDO files are generated from the Quartus II software.

Sample Prime Time Timing Report

This section presents a sample timing report.

Table 5-2. Sample Prime Time Timing Report		
Startpoint: ~I.out_reg (rising edge-triggered flip-flop clocked by clk)		
Endpoint: out (output port clocked by clk)		
Path Group: clk		
Path Type: max		
Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (propagated)	2.362	2.362
out~I.out_reg.clk (stratix_io_register)	0.00	2.362 r
out~I.out_reg.regout (stratix_io_register)	0.162*	2.524 r
out~I.out_mux3.MO (mux21)	0.000	2.524 r
out~I.and2_22.Y (AND2)	0.000	2.524 r
out~I.out_mux1.MO (mux21)	0.000	2.524 r
out~I.inst1.padio (stratix_asynch_io)	2.715H	5.239 r
out~I.padio (stratix_io)	0.000	5.239 r
out (out)	0.00	5.239 r
data arrival time		5.239 r
clock clk (rise edge)	10.000	10.000
clock network delay (propagated)	0.000	10.000
output external delay	-7.000	3.000
data required time		3.000
data required time		3.000
data arrival time		-5.239
slack (VIOLATED)		-2.239

The start point in this report is a register clocked by `clock`, `clk`. Endpoint is an output pin, `out`. This is equivalent to either a `tCO` or a Minimum `tCO` path in the Quartus II software, depending on the `-delay` option. At the end of the report, "Violated" is listed, which means that the constraint was not met. A negative slack is also given, as it is in the Quartus II software.

Running Prime Time

Prime Time is only available to run on Unix systems. The three files created by the Quartus II software must be transferred to a Unix machine. Prime Time runs in shell mode by accepting scripts in Tcl format. The `<project_name>_pt_v.tcl` script file, for example, is executed in the following way:

Type the following command at the UNIX command line prompt, and press the Return key:

```
pt_shell -f project_name_pt_v.tcl
```

After all commands in the Tcl script file are executed, "pt_shell>" prompt appears. More `pt_shell` commands can be executed at that prompt, including the following:

- `man report_timing`

This command lists details of how to use the `report_timing` command and all related options.

- `help`

Entering this command at the `pt_shell` prompt lists all the commands available in the `pt_shell`.

- `quit`

Entering this command at the `pt_shell` prompt closes the `pt_shell`.

You can also activate `pt_shell` without a script file by entering `pt_shell` at the UNIX command line prompt.

Conclusion

The Quartus II-generated netlist, constraints, and timing information can be exported into the Prime Time environment seamlessly. Prime Time can be used to do worst-case and best-case timing analysis just as in the Quartus II software. Prime Time timing reports show any violations and slacks.