

Introduction

As designs grow larger and processes continue to shrink, power becomes an ever-increasing concern. When designing a printed circuit board (PCB), the power consumed by a device needs to be accurately estimated to develop an appropriate power budget and to design the power supplies, voltage regulators, heat sink and cooling system. Stratix™, Stratix GX, and Cyclone™ device power consumption can be calculated using the Microsoft Excel (Excel)-based power calculator or the Simulation-Based Power Estimation feature in the the Quartus® II software, which is described in the *Simulation-Based Power Estimation* chapter in Volume 3 of the *Quartus II Handbook*.

You can use the Excel-based power calculator during the board design and layout phase to estimate power and design for proper power management. While you can also use the simulation-based power estimation feature in the Quartus II software when simulation vectors are available to verify that your design is within your power budget.

Excel-Based Power Calculator

An Excel-based power calculator, which provides a current (I_{CC}) and power (P) estimation based on typical conditions (room temperature and nominal V_{CC}), is available on the Altera website for Stratix, Stratix GX and Cyclone devices. The power calculator is divided into sections, with each section representing an architectural feature of the device, such as the clock network, RAM blocks, or digital signal processing (DSP) blocks. You must enter the device resources, operating frequency, toggle rates, and other parameters in the power calculator to estimate the device power consumption. The sub-total of the I_{CC} and power consumed by each architectural feature is reported in each section in milliamps (mA) and milliwatts (mW), respectively.

Before reading this chapter, you should be familiar with the Excel-based Stratix, Stratix GX, or Cyclone power calculators available on the Altera website.



For more information about how to use the Excel-based power calculator, see the *Estimating Power in Stratix, Stratix GX, and Cyclone Devices User Guide*.

Figures 6–1 through 6–5 show sections of the Stratix power calculator.

Figure 6–1. Device and I_{CC} Standby Sections in the Stratix Power Calculator


 www.altera.com		Altera® Stratix™ Device Power Calculator Spreadsheet Version 2.3 Altera does not guarantee or imply the reliability, serviceability, or function of this Program or other items provided as part of this Program. The files contained herein are provided 'AS IS'. ALTERA DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Copyright Altera Corporation. All rights reserved.				
		Comments:				
Device						
Device	Package	Temperature Grade	V _{CCINT}	Total P _{INT} (mW)	Total P _{IO} (mW)	Total P (mW)
EP1K25	780 FineLine BGA	C - commercial	1.5-V	135.00	0.00	135.00
I_{CC} Standby (mA)						
Typical	90	Clear All Values				

Figure 6–2. Clock Network Section in the Stratix Power Calculator

Clock Network				
Global Clock Network	f _{MAX} (MHz)	# Flip-Flops	I _{CCINT} (mA)	P _{INT} (mW)
1	100	984	32.21	48.31
2	20	19	0.43	0.65
3	250	2006	135.97	203.95
4	100	1792	50.09	75.14
5	5	152	0.49	0.74
Subtotal			219.19	328.78
Regional Clock Network	f _{MAX} (MHz)	# Flip-Flops	I _{CCINT} (mA)	P _{INT} (mW)
1	50	398	6.18	9.27
2	10	2800	5.06	7.59
Subtotal			11.24	16.86
Fast Regional Clock Network	f _{MAX} (MHz)	# Flip-Flops	I _{CCINT} (mA)	P _{INT} (mW)
1	156	1109	41.85	62.77
Subtotal			41.85	62.77

Figure 6–3. Logic Elements Section in the Stratix Power Calculator

Logic Elements (LEs)						
Average Fan-out						
4.16						
Design Module	f _{MAX} (MHz)	# LEs	# LEs w/Carry	Toggle %	I _{CCIR} (mA)	P _{WR} (mW)
1	250	2500	2000	12.50	86.06	129.08
2	100	1700	1400	12.50	23.53	35.30
3	50	500	400	12.50	3.44	5.16
4	20	511	421	12.50	1.41	2.12
5	10	600	450	12.50	0.82	1.23
6	0	0	0	0.00	0.00	0.00
7	0	0	0	0.00	0.00	0.00
8	0	0	0	0.00	0.00	0.00
9	0	0	0	0.00	0.00	0.00
10	0	0	0	0.00	0.00	0.00
Subtotal					115.26	172.89

Figure 6–4. RAM Blocks Section in the Stratix Power Calculator

RAM Blocks										
M512 Blocks										
Design Module	f _{MAX} (MHz)	# Data Inputs	# Data Outputs	Toggle %	# M512 Blocks Used	Mode	Total I _{CC_READ}	Total I _{CC_WRITE}	I _{CCIR} (mA)	P _{WR} (mW)
1	100	3	3	12.50	50	Single-Port	0.47	2.73	11.20	16.80
M4K Blocks										
Design Module	f _{MAX} (MHz)	# Data Inputs	# Data Outputs	Toggle %	# M4K Blocks Used	Mode	Total I _{CC_READ}	Total I _{CC_WRITE}	I _{CCIR} (mA)	P _{WR} (mW)
1	100	0	8	12.50	20	ROM	4.63	0.00	4.63	6.94
M-RAM Blocks										
Design Module	f _{MAX} (MHz)	# Data Inputs	# Data Outputs	Toggle %	# M-RAM Blocks Used	Mode	Total I _{CC_READ}	Total I _{CC_WRITE}	I _{CCIR} (mA)	P _{WR} (mW)
1	100	48	48	12.50	2	Two-Port	2.55	0.19	2.74	4.11

Figure 6–5. General I/O Power Section in the Stratix Power Calculator

General I/O Power							
Design Module	f _{MAX} (MHz)	# Outputs & Bidirectional Pins	Toggle %	Avg. Capacitive Load (pF)	I/O Standard	I/O Data Rate	I _{CCIO} (mA)
1	156	64	25.00	4	LVDS	SDR	250.07
2	133	55	12.50	8	3.3-V PCI	SDR	52.65
3	50	80	12.50	20	3.3_LVTTTLVCMOS_24	SDR	42.55
4	66	128	12.50	10	SSTL-16_L	SDR	561.11

Estimating Power in the Design Cycle

You can estimate power at different stages of your design cycle. Depending where you are in your design cycle, you can either use the Excel-based power calculator or the simulation-based power estimation feature in Quartus II.

Since FPGAs provide the convenience of a shorter design cycle and faster time-to-market, the board design often takes place during the FPGA design cycle, which means the power planning for the device can happen before the FPGA design is complete. If the FPGA design has not yet

begun, or is not complete, an estimate of the power consumption for the design can be made using the Excel-based power calculator. [Table 6-1](#) shows the power estimation flow when using the Excel-based power calculator when the FPGA design has not begun.

Table 6-1. Power Estimation Before FPGA Design Has Begun

Steps to Follow	Advantages	Disadvantages
1. Download the Excel-based power calculator from the Altera website	Power Estimation can be done before any FPGA design is complete	Accuracy is dependent on user input and estimate of the device resources
2. Manually fill in the power calculator		Can be time consuming

When the FPGA design is partially complete, the power estimation file generated by the Quartus II software can help to fill in the Excel-based power calculator. After using the Import Data macro to import the power estimation file information into the Excel-based power calculator, you can edit the power calculator to reflect the device resource estimates for the final design.



For more information about how to generate the power estimation file in the Quartus II software, see [“Quartus II Power Report File”](#) on page 6-6.



For more information about how use the Import Data macro to import the power estimation file information into the Excel-based power calculator, see the *Estimating Power in Stratix, Stratix GX, and Cyclone Devices User Guide*.

Table 6–2 shows the power estimation flow for the Excel-based power calculator when the FPGA design is partially complete.

Table 6–2. Power Estimation When FPGA Design Is Partially Complete

Steps to Follow	Advantages	Disadvantages
1. Compile the partial FPGA design in the Quartus II software	Power Estimation can be done early in the FPGA design cycle Provides the flexibility to automatically fill the power-calculator based on results of compilation in the Quartus II software	Accuracy is dependent on user input and estimate of the final design device resources
2. Generate the Power Estimation File in the Quartus II software		
3. Download the Excel-based power calculator from the Altera website		
4. Run the import data macro to automatically populate the Excel-based power calculator		
5. Optionally, edits to the power calculator can be made to reflect the device resources used in the final design		

When the FPGA design is complete, the device power consumption can be estimated with the simulation-based power estimation feature in Quartus II. The Quartus II Simulator provides simulation-based power estimation for Stratix, Stratix GX, Cyclone, HardCopy™ Stratix, MAX® 7000AE, MAX 7000B, and MAX 3000A devices. To use the power estimation feature, you must provide a Vector Waveform File (.vwf) or Power Input File (.pwf) to the Quartus II Simulator and perform a timing simulation.



For more information about how to use the simulation-based power estimation feature in the Quartus II software, see the *Simulation-Based Power Estimation* chapter in Volume 3 of the *Quartus II Handbook*.

Table 6–3 shows the power estimation flow for the simulation-based power estimation feature in the Quartus II software when the FPGA design is complete.

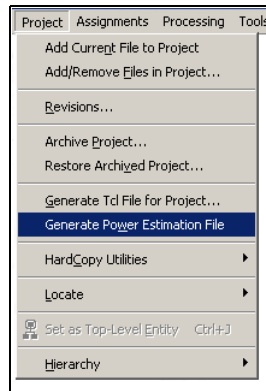
Table 6–3. Power Estimation When FPGA Design Is Complete		
Steps to follow	Advantages	Disadvantages
1. Compile the FPGA design in Quartus II	Provides the most accurate power estimation since the simulation stimuli reflects actual device behavior	Power Estimation done later in the FPGA design cycle
2. Create the stimulus for simulation		
3. Simulate the design using Quartus II vector files or a Power Input File (.pwf) from a third party simulation tool		
4. Quartus II Simulator reports the power estimation results		

Quartus II Power Report File

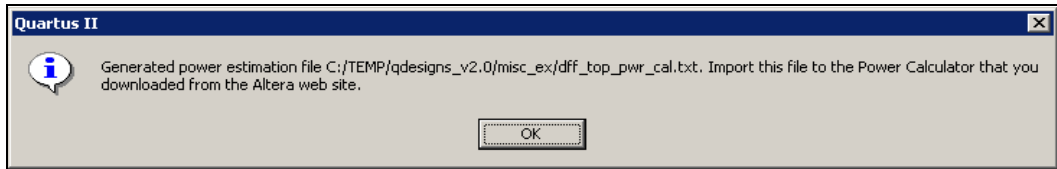
When filling out the Excel-based power calculator, you enter the device resources, operating frequency, toggle rates and other parameters in the power calculator. This requires familiarity with the design. If you do not have an existing design, then you must estimate the number of device resources used in your design.

If you already have an existing design or a partially completed design, the power estimation report file that is generated by the Quartus II software version 4.0 can aid in filling out the power calculator.

To generate the power estimation file, you must first compile your design in the Quartus II software version 4.0. After compilation is complete, choose **Generate Power Estimation File** (Project menu), which instructs the Quartus II software to write out a power estimation report text file. See Figure 6–6.

Figure 6–6. Generate Power Estimation File Option

After the Quartus II software successfully generates the power estimation report file, a message is displayed. See [Figure 6–7](#).

Figure 6–7. Generate Power Estimation File Message

The power estimation report file is named *<name of Quartus II project>_pwr_cal.txt*. [Figure 6–8](#) is an example of the contents of a power estimation file generated by the Quartus II software version 4.0.

Figure 6–8. Example of Power Estimation File

```
Power Estimation File for dff_top - Do not edit this
line

<name=DEVICE value=EP1S25F780C5>

<name=fmax_RC1 value=100>
<name=ff_RC1 value=984>
<name=fmax_LE1 value=100>
<name=tot_LE1 value=1700>
<name=totwcc_LE1 value=1400>
<name=fmax_GIO1 value=50>
<name=NumbOB_GIO1 value=80>
<name=avgCLoad_GIO1 value=20>
<name=iostd_GIO1 value=3.3_LVTTL/LVCMOS_24>
<name=iodatarate_GIO1 value=SDR>
```

The Stratix Power Calculator v2.4, Stratix GX Power Calculator v1.3, and Cyclone Power Calculator v1.2 power calculation spreadsheets include the Import Data macro that parses the information in the power estimation file and transfers it into the Excel-based power calculator. If you do not want to use the macro, you can also transfer the data into the Excel-based power calculator manually.

If your existing Quartus II project represents only a portion of your full design, you should manually enter in the additional resources that are used in the final design. Therefore, after importing the power estimation file information into the Excel-based power calculator, you can edit it to add in additional device resources.



For completed designs, see the *Simulation-Based Power Estimation* chapter in Volume 3 of the *Quartus II Handbook*.

Conclusion

The power calculator is an easy and useful tool to estimate the power consumption for your designs based on typical conditions. The power estimation file generated by the Quartus II software helps to fill in the Excel-based power calculator available on the Altera website. Board-level and FPGA designers can benefit from the power estimation report file generated by the Quartus II software to more accurately estimate power.

References

Estimating Power in Stratix, Stratix GX, and Cyclone Devices User Guide