



March 2004

## Handbooks

### *HardCopy Handbook*

#### Section I. HardCopy Stratix Device Family Data Sheet

Chapter 1. Introduction

Chapter 2. Description, Architecture & Features

Chapter 3. Design Migration Flow

Chapter 4. Boundary-Scan Support

Chapter 5. Operating Conditions

#### Section II. HardCopy APEX 20K Device Family Data Sheet

Chapter 6. Introduction

Chapter 7. Description Architecture & Features

Chapter 8. Design Migration Flow

Chapter 9. Boundary-Scan Support

Chapter 10. Operating Conditions

#### Section III. Hardware Design Considerations

Chapter 11. Design Guidelines for HardCopy Migration

Chapter 12. Configuration Emulation in HardCopy Devices

Chapter 13. Timing Closure for HardCopy Devices

#### Section IV. Software Support

Chapter 14. Quartus II Support for HardCopy Devices

## Data Sheets *Note (1)*

Altera Device Package Information Data Sheet

ARM-Based Embedded Processor Device Overview Data Sheet

Configuration Devices for FLEX & APEX Devices Data Sheet Version 10

Cyclone FPGA Family Data Sheet

fft Fast Fourier Transform Data Sheet

APEX 20K Programmable Logic Device Family Data Sheet

FLEX 10KE Embedded Programmable Logic Family Data Sheet

FLEX 10K Embedded Programmable Logic Family Data Sheet  
FLEX 10K PCI Prototype Board Data Sheet  
FLEX 6000 Programmable Logic Device Family Data Sheet  
HardCopy Devices for APEX 20K Conversion  
MasterBlaster Serial/USB Communications Data Sheet  
MAX 9000 Programmable Logic Device Family Data Sheet  
MAX 7000 Programmable Logic Device Family Data Sheet  
MAX 7000A Programmable Logic Device Family Data Sheet  
MAX 7000B Programmable Logic Device Family Data Sheet  
MAX+PLUS II Programmable Logic Development System & Software Data Sheet  
Mercury Programmable Logic Device Family Data Sheet  
MIPS-Based Embedded Processor Device Overview Data Sheet  
Nios Embedded Processor SPI Peripheral Data Sheet  
Nios Embedded Processor Timer Peripheral Data Sheet  
Nios Embedded Processor UART Peripheral Data Sheet  
Nios Soft Core Embedded Processor Data Sheet  
Operating Requirements for Altera Devices Data Sheet  
PCI Master/Target MegaCore Function with DMA Data Sheet  
pci\_b PCI Master/Target MegaCore Function Data Sheet  
pcit1 PCI Target MegaCore Function Data Sheet  
SignalTap Embedded Logic Analyzer Megafunction Data Sheet  
Serial Configuration Devices Data Sheet  
Stratix FPGA Family Data Sheet

### **Application Notes**     *Note (1)*

AN 42    Metastability in Altera Devices  
AN 71    Guidelines for Handling J-Lead & QFP Devices  
AN 74    Evaluating Power for Altera Devices  
AN 75    High-Speed Board Designs  
AN 80    Selecting Sockets for Altera Devices  
AN 81    Reflow Soldering Guidelines for Surface-Mount Devices  
AN 88    Using the Jam Language for ISP via an Embedded Processor  
AN 91    Understanding FLEX 10K Timing  
AN 92    Understanding FLEX 6000 Timing  
AN 94    Understanding MAX 7000 Timing

- AN 96 Performance Measurements of Typical Applications
- AN 97 Comparing Performance of High-Density PLDs
- AN 100 In-System Programmability Guidelines
- AN 101 Improving Performance in FLEX 10K Devices with the Synplify Software
- AN 102 Improving Performance in FLEX 10K Devices with Leonardo Spectrum Software
- AN 106 Designing with 2.5-V Devices
- AN 110 Gate Counting Methodology for APEX 20K Devices
- AN 112 Integrating Product-Term Logic in APEX 20K Devices
- AN 114 Designing with FineLine BGA Packages
- AN 115 Using the ClockLock & Clock Boost Features in APEX Devices
- AN 116 Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices
- AN 117 Using Selectable I/O Standards in Altera Devices
- AN 118 Scripting with Tcl in the Quartus Software
- AN 119 Implementing High-Speed Search Applications with APEX CAM
- AN 122 Using Jam STAPL for ISP & ICR via an Embedded Processor
- AN 123 Using Timing Analysis in the Quartus Software
- AN 125 Evaluating AMPP & MegaCore Functions
- AN 129 Implementing a W-CDMA System with Altera Devices & IP Functions
- AN 130 CDR in Mercury Devices
- AN 131 Using General Purpose PLLs in Mercury Devices
- AN 132 Implementing Multiprotocol Label Switching with Altera PLDs
- AN 161 Using the LogicLock Methodology in the Quartus II Design Software
- AN 202 Using High-Speed Differential I/O Interfaces in Stratix Devices
- AN 205 Understanding Altera Software Licensing
- AN 229 Advanced Troubleshooting for Altera Software Licensing
- AN 250 Configuring Cyclone FPGAs
- AN 251 Using PLLs in Cyclone Devices
- AN 252 On-Chip Memory Implementation Using Cyclone Memory Blocks
- AN 253 Using Selectable I/O Standards in Cyclone Devices
- AN 255 Guidelines to Migrating Spartan Designs to Cyclone Designs
- AN 256 Implementing Double Data Rate I/O Signaling in Cyclone Devices
- AN 258 Using Cyclone Devices in Multi-Voltage Systems

## **Brochures**     *Note (1)*

ACEX Device Brochure

APEX Device Brochure  
APEX II Device Brochure  
Automotive Solutions Brochure  
Cyclone Device Brochure  
Excalibur Brochure  
FLEX 10K Brochure  
FLEX 6000 Brochure  
HardCopy Brochure  
Lead-Free Packaging Brochure  
MAX Device Brochure  
MegaCore Functions Brochure  
Mercury Device Brochure  
Signal Processing IP Megafunctions Brochure  
Stratix Device Brochure  
Stratix GX Device Brochure

### Product Information Bulletins

PIB 29 LVDS Comparison APEX 20KE vs. Virtex-E Devices

### Selector Guides *Note (1)*

Component Selector Guide  
Design Software & Development Kit Selector Guide  
Intellectual Property Selector Guide

### Solution Briefs *Note (1)*

SB 6 PCI Bus Target Megafunction  
SB 17 Early/Late Gate Synchronizer Megafunction  
SB 19 EC210 PCI Bus Master/Target Megafunction  
SB 20 PCI Bus Master/Target MegaCore Function  
SB 21 a8259 Programmable Interrupt Controller MegaCore Function  
SB 22 CAN Bus Megafunction  
SB 24 USB Function Controller Megafunction  
SB 25 PCI Bus Target Interface Megafunction  
SB 26 PCI Bus Master/Target Interface Megafunction

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SB 28	USB Host Controller Megafunction
SB 30	crc MegaCore Function Parameterized CRC Generator/Checker
SB 32	Telephony Tone Generation Megafunction
SB 33	Viterbi Decoder Megafunction
SB 34	IDR Deframer Megafunction
SB 35	ATM Cell-Based UTOPIA Level 1 Interface Megafunction
SB 36	IEEE 1394-Compatible LLC-I Megafunction
SB 39	I2C Master Interface Megafunction
SB 40	I2C Slave Interface Megafunction
SB 41	FIR Compiler MegaCore Function
SB 42	Interleaver/Deinterleaver MegaCore Function
SB 44	64-Bit PCI Master/Target MegaCore Function
SB 46	FLEX PCI Development Kit
SB 47	System-on-a-Programmable-Chip (SOPC) Development Board
SB 48	Reed-Solomon Compiler MegaCore Function
SB 49	NCO Compiler MegaCore Function
SB 50	Turbo Encoder/Decoder MegaCore Function
SB 55	APEX 20KE PCI Starter & Development Kit

## Technical Briefs *Note (1)*

TB 3	FLEX Devices as Alternatives to ASSPs & ASICs
TB 4	Using FLEX Devices as DSP Coprocessors
TB 15	Implementing a 100,000-Gate Gate Array Design in an EPF10K100 Device
TB 24	The Advantages of LPM
TB 25	Using the OpenCore Evaluation Feature
TB 26	FLEX 10K & pci_a: The Complete PCI Solution
TB 28	Advantages of ISP-Based CPLDs
TB 30	Authorization Codes Now Via the WWW
TB 32	ISP Programming Methods & Ordering Codes
TB 33	Evaluating MAX 7000S Device Utilization & Fitting
TB 34	MAX 7000S Power Consumption
TB 36	Timing-Driven Compilation Improvements in MAX+PLUS II Version 8.2
TB 38	FLEX 10KA-1 Devices: The Fastest High-Density Devices Available
TB 39	Using Synopsys Design Compiler & FPGA Compiler to Synthesize Designs for MAX+PLUS II Software

TB 41	Power Measurements: FLEX 10KA vs. XC4000 Devices
TB 42	Using Synopsys FPGA Express Software to Synthesize Designs for MAX+PLUS II Software
TB 44	Using Synplicity Synplify Software to Synthesize Designs for MAX+PLUS II Software
TB 45	Importing Synthesized Files from EDA Tools into the MAX+PLUS II Software for Place & Route
TB 48	Passing Hierarchical Timing Constraints from Synopsys Tools to MAX+PLUS II Version 9.0
TB 51	Advantages of Quartus Internet Integration
TB 57	Power Consumption Comparison: APEX 20K vs. Virtex Devices
TB 60	Advantages of APEX PLLs over Virtex DLLs
TB 61	CAM Comparison: APEX 20KE vs. Virtex-E Devices
TB 70	Jitter Comparison Analysis: APEX 20KE PLL vs. Virtex-E DLL
TB 78	APEX II Clock-Data Synchronization (CDS) Competitive Advantage

## User Guides & Manuals

FIR Compiler MegaCore Function User Guide  
Nios Embedded Processor Programmer's Reference Manual  
Reed-Solomon Compiler MegaCore Function User Guide  
Symbol Interleaver/De-Interleaver MegaCore Function User Guide  
Introduction to Quartus II Manual

## White Papers *Note (1)*

Configuring PLDs with FLASH Memory White Paper  
Designing Switches & Routers with APEX CAM White Paper  
Excalibur Backgrounder White Paper  
Implementing Quality of Service with Altera PLDs White Paper  
Using Altera's 1.0-mm FineLine BGA Packages White Paper  
Using I/O Standards in the Quartus Software White Paper  
Using LVDS in APEX 20KE Devices White Paper  
Using MAX 7000B Devices to Replace I/O Drivers White Paper

### **Note:**

- (1) To view Japanese text, you must be running the Japanese version of Acrobat Reader with the Asian language plug-in. You can download the Japanese version of Acrobat Reader from the Adobe web site.