



# Quartus II Software Release Notes

July 2002

Quartus II version 2.1

This document provides late-breaking information about the following areas of this version of the Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **quartus** directory.

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## New Features & Enhancements

The Quartus® II software version 2.1 includes a new timing closure methodology. This timing closure methodology is facilitated by a suite of features that allows you to achieve timing requirements on all clock signals in your hardware design with fewer iterations. Altera® is the first programmable logic supplier to develop and deliver an integrated timing closure methodology at no additional cost. Commonly used in multimillion gate ASIC designs, timing closure methodologies are a fundamental requirement for high complexity digital design.

Additionally, version 2.1 of the Quartus II software provides enhancements and improvements in PLD design, embedded software design, the LogicLock™ block-based design flow, fitting, verification, and device support.

### Design

- Device and EDA tool settings are now integrated in the **New Project Wizard**.
- Device migration is supported for APEX™ II, APEX™ 20K, APEX 20KE, APEX 20KC, and MAX® 7000 device families.
- HardCopy™ device Design Assistant checks designs to make sure they can be migrated easily to low-cost, high-volume HardCopy devices.
- Tool command language (Tcl) scripts can be accessed on the new Tcl toolbar.
- Information and warning messages can be suppressed during compilation, simulation, or software building.

### Embedded Software Design

- The SOPC Builder system development tool is now integrated with the Quartus II user interface with support for Excalibur™ devices in addition to the Nios® embedded processor.
- The Red Hat GNUPro C/C++ development tools are provided with Altera subscriptions.
- **MegaWizard® Plug-In Manager** support for Excalibur devices has been added for HP-UX 11.0 and Linux operating systems.

### LogicLock Block-Based Design Flow

- Support for virtual I/O pins allows users to map LogicLock™ I/O pins to internal nodes in the top-level design.
- Soft region support allows you to place nodes outside a LogicLock region in order to meet timing requirements.
- The Project Navigator now displays resource entity usage for LogicLock regions.

## Fitting

- The new timing closure methodology includes the Timing Closure Floorplan, the ability to make path-based assignments, new netlist optimizations, and incremental, block-based placement.
- The **Initial Placement Configuration** option provides an average 5% performance increase by applying different starting values for place and route.
- The Fitter now automatically packs registers into DSP blocks for ~4% performance improvement.
- The Fitter now uses improved logic element register packing algorithms to reduce run times and improve routing resource usage.

## Verification

- Introduction of the SignalTap<sup>®</sup> II Embedded Logic Analyzer.
- Excalibur Stripe Simulator (ESS) quickly simulates ARM<sup>®</sup> processor, PLD, internal and external memory, and peripherals simultaneously.
- SignalProbe<sup>™</sup> support for Stratix EP1S25 devices.
- Improved SignalProbe routing success rate for APEX 20K, APEX II, and Excalibur device families.
- PowerGauge<sup>™</sup> support for the APEX II and Excalibur device families.
- Updated PowerGauge support for Mercury<sup>™</sup> devices.
- Support for Atrenta Spyglass and Synopsys LEDA design rule-checking tools.

## Online Help

- Links to other Altera documentation on the World Wide Web, such as Application Notes are now available from selected Help topics.
- The navigation in the EDA section of Quartus II Help has been modified to improve accessibility to EDA-related topics.
- The LogicLock Tutorial is enhanced to include information about the Timing Closure Floorplan feature.

# Device Support & Pin-Out Status

## Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

### *Devices with Full Support*

Device Family	Devices	
MAX 3000A	EPM3512A Q208	EPM3512A F256
Stratix	EP1S25 F780	EP1S25 B672
	EP1S25 F672	EP1S25 F1020

## Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although pin-out information is generated by the Compiler, programming files are not generated for these devices in this release.

### *Devices with Advance Support*

Device Family	Devices
Stratix	EP1S30 F789

## Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

### *Devices with Initial Information Support*

Device Family	Devices
None	

## Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

### Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

#### *Devices with Preliminary Timing Models*

Device Family	Device	Notes
Stratix	EP1S10	The Quartus II software version 2.1 includes preliminary timing models for -5, -6, and -7 speed grades for the Stratix device family.
	EP1S20	
	EP1S25	
	EP1S30	
	EP1S40	
	EP1S60	
	EP1S80	
	EP1S120	

### Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

#### *Devices with Final Timing Models*

Device Family	Device	Timing Models Final in Quartus II Version No.
APEX II	EP2A15	2.1
	EP2A25	2.1
	EP2A40	2.1
	EP2A70	2.1
APEX 20KC	EP20K200C	
	EP20K400C	2.0
	EP20K600C	2.0
	EP20K1000C	
Excalibur	EPXA1	2.0 SP1
	EPXA4	2.0 SP1
	EPXA10	2.0 SP1

Device Family	Device	Timing Models Final in Quartus II Version No.
Mercury	EP1M350 (copper)	2.0
	EP1M120 (aluminum)	
	EP1M120 (copper)	
MAX 7000	EPM7032AE	2.0
	EPM7064AE	2.0
	EPM7128AE	2.0
	EPM7256AE	2.0
	EPM7512AE	2.0
	EPM7032B	2.0
	EPM7064B	2.0
	EPM7128B	2.0
	EPM7256B	2.0
MAX 3000	EPM3032A	2.0
	EPM3064A	2.0
	EPM3128A	2.0
	EPM3256A	2.0

This version of the Quartus II software also includes final timing models for the APEX 20KE, FLEX 10K, ACEX 1K, and the FLEX 6000 device families. Final timing models for these device families became final in versions earlier than version 2.0.

## EDA Interface Information

The Quartus II software version 2.1 supports the following EDA tools.

### **Supported EDA Tools**

Synthesis Tools	Version	NativeLink support
Mentor Graphics® LeonardoSpectrum™-Altera	2002c	✓
Mentor Graphics® LeonardoSpectrum™	2002c	✓
Synopsys Design Compiler	2001.08	
Synopsys FPGA Compiler II	3.7	✓
Synplicity® Synplify® and Synplify Pro®	7.1A	✓
ADT PALACE	2.1	✓

Verification Tools	Version	NativeLink support
Cadence NC-Verilog	3.3	✓
Cadence NC-VHDL	3.3	✓
Cadence Verilog-XL	3.3	
Model Technology™ ModelSim®	5.6a	✓
Model Technology ModelSim-Altera	5.6a	✓
Innoveda BLAST	1.2.2	
Synopsys PrimeTime	2000.05	✓
Synopsys Scirocco	2000.12	✓
Synopsys VSS	2000.05	
Synopsys VCS	6.0	
Mentor Graphics Tau	2.2	
Verplex Conformal LEC	3.1.0a	

## Known Issues & Workarounds

### General Quartus II Software Issues

Issue	Workaround
Versions of the Quartus II software earlier than version 2.0 cannot open Block Design Files (.bdf) created with the Quartus II software version 2.0 and later.	
Within each device family, not all speed grades of a given device share the same features.	Refer to the Altera data sheet for the device family for further information.

Issue	Workaround
<p>There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.</p>	<p>Connect the port to a top-level bidirectional pin or to other logic in the design.</p>
<p>To use the EP20K400GC655 device in your design, please contact the Altera Customer Applications Department.</p>	
<p>Registers that feed output pins will have the same name as the output pin when you view the post-fitting register names.</p>	
<p>If you have a version of the Quartus® software previous to the Quartus II software version 1.0 installed on your computer in addition to the Quartus II software, you must start the previous version of the program by running the <b>runq.exe</b> program from the <b>\quartus\bin</b> directory containing the previous version you wish to use.</p>	
<p>If you compile a design with the <b>Run batch simulation</b> option turned on and, once compilation has completed, click on any simulation waveform in the Simulation Report window and then choose <b>Simulate Mode</b> (Processing menu), an error may occur.</p>	<p>Close the Simulation Report window before changing to Simulate mode.</p>

Issue	Workaround
<p>The PowerFit™ Fitter supports assignments to LAB cliques only. Back-annotating a design containing assignments to other types of cliques may create illegal assignments that result in a “no fit.”</p>	<p>Remove all assignments to cliques before recompiling a back-annotated design.</p>
<p>You should not create multiple Compiler settings that have the same design entity as the “compilation focus.”</p>	
<p>The command-line version of the Quartus II software does not accept a path name as part of the project name.</p>	<p>Run the Quartus II software from the directory where your project is stored.</p>
<p>Under some circumstances, if the <b>Optimize I/O cell register placement for timing</b> option in the <b>Compiler Settings</b> dialog box (Processing menu) is turned on and you are using multiple peripheral clock enable signals, you may receive an error message or the Quartus II software may crash.</p>	<p>Set the <b>Clock Enable Routing</b> logic option to “Single-Pin” for some of the clock enable signals.</p>
<p>Context-sensitive Help is not available for some items in the Quartus II software.</p>	<p>To locate Help on those items, choose <b>Index</b> from the Help menu and type the name of the item.</p>

Issue	Workaround
<p>The Quartus II software provides limited support for the following I/O standards for APEX™ 20KE devices that are not available with the <b>I/O Standard</b> logic option:</p> <ul style="list-style-type: none"> <li>• <b>LVPECL</b> is a differential I/O standard similar to LVDS. APEX 20KE devices can support LVPECL I/O pins by using the I/O pins in LVDS mode with an external resistor network.</li> <li>• <b>PCI-X</b> is an enhanced version of the <b>PCI</b> I/O standard that can support a higher average bandwidth. This standard has more stringent requirements than <b>PCI</b>.</li> </ul>	<p>To use the <b>LVPECL</b> I/O standard in APEX 20KE devices in the Quartus II software, set the <b>I/O Standard</b> logic option for the pins to <b>LVDS</b> and connect the pins to an appropriate external resistor network.</p> <p>The APEX 20KE I/O drivers meet the requirements for <b>PCI-X</b>. Turn on the <b>PCI I/O</b> logic option to support <b>PCI-X</b> requirements, including the overshoot clamp.</p>
<p>You cannot locate an error in a design file if compilation was unsuccessful due to a syntax error.</p>	
<p>If you open a project that was created using a previous version of the Quartus II software, you may receive a message that indicates that the database is incompatible and that results of the last compilation will be lost.</p>	<p>Back-annotate all of the project assignments in the previous version. Then, delete the \<i>project name</i>\db directory and all of its contents.</p>
<p>The Timing Analyzer does not recognize non-PLL clock signals when using the <code>altclklock</code> megafunction.</p>	<p>Make <b>Clock Settings</b> assignments to all non-PLL clocks.</p>
<p>If you are using the <code>lpm_mult</code> megafunction, you must turn off the <b>Auto Cascade Chains</b> option when editing project defaults in the <b>Parameters</b> tab of the <b>Option &amp; Parameter Settings</b> dialog box (Project menu).</p>	

Issue	Workaround
The Waveform editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create busses only with nodes that are consecutive members of a bus. Or, use the <b>Group</b> command (Edit menu) to create groups of arbitrary nodes.
Using the <b>Cancel</b> button in the Assignment Organizer when multiple nodes have been selected, causes the Quartus II software to restore the setting of the first node to all the nodes that were edited.	Do not use the <b>Cancel</b> button to cancel changes made to two or more selected nodes that have assignments of differing settings.
If you are using the <code>altcam</code> , <code>altclklock</code> , <code>altlvds_rx</code> , or <code>altlvds_tx</code> megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Last Compilation floorplan.
The Quartus II software does not support file names with more than one extension. For example, you cannot use the file name <b>file.eda.edif</b> .	Use file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files also on the network.	Altera recommends using versions 1.9.16p11 and 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation ( <code>debug[7..0]</code> ), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying “Unsupported data type in the top-level module.”	Reserve the pins using single name notation (e.g., <code>debug7</code> , <code>debug6</code> , and so on).

Issue	Workaround
<p>The Quartus II software version 2.1 supports only version 5.2 and later of the PowerKit™ software. Previous versions of the PowerKit software are not supported with this version of the Quartus II software.</p>	
<p>Under some circumstances, an error message saying “Can’t start server. Beginning attempt 1/3...” appears when starting a compilation, simulation, or software build.</p>	<p>Increase the value of the environment variable <code>QUARTUS_PROCESS_TIMEOUT</code> from the default value of 100. If the environment variable does not exist, set it to an initial value of 200. You may have to increase the value until you no longer receive the error message.</p>
<p>If you are using the HSTL Class II I/O standard with an APEX II device, additional information is required.</p>	<p>Contact the Altera Customer Applications department at <a href="mailto:apexii@altera.com">apexii@altera.com</a> for information about Service Packs and device pin-outs.</p>
<p>In the Package view in the Floorplan Editor, all <code>GND_IO</code> pins for APEX, APEX E, and APEX II devices are incorrectly shown as being in Bank 9.</p>	<p>Ignore the I/O bank information, the <code>GND_IO</code> pins are not associated with any I/O bank.</p>
<p>Do not change the file permissions (such as changing read-only to read and write) of Quartus II settings and configurations files (<code>.csf</code>, <code>.esf</code>, etc.) while a Quartus II project is open.</p>	<p>Close your Quartus II project before making changes to the file permissions.</p>
<p>The order of ports for the <b>ARM-based Excalibur MegaWizard</b>-generated symbol for the stripe changed in version 2.0 of the Quartus II software. If you re-run the MegaWizard for a design created in a version of the Quartus II software earlier than version 2.0, you will receive port connection errors when you compile the design.</p>	<p>To avoid receiving these errors, adjust the port connections in the Block Design File (<code>.bdf</code>) after updating the symbol.</p>

Issue	Workaround
Node names containing numbers greater than $2^{31}-1$ (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
When you are using STAPL Jam/JBC to configure an Excalibur device, a syntax error occurs when the processor stripe fails to be configured instead of an error message indicating the failure.	
When you are using STAPL Jam/JBC to configure multi-device chains, you may receive a report that the configuration of the chain failed when it actually succeeded.	
Occasionally the Programmer does not allow you to use a MAX 7000AE POF with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
If you are using EPC 4/8/16 devices in a chain, you must turn on the <b>Examine</b> option only for the EPC 4/8/16 device(s) in the chain. If you turn on the Examine option for devices other than the Configuration devices, an error will result.	Turn on the <b>Examine</b> option for all EPC 4/8/16 devices in the chain, or bypass the devices not being examined.
The Quartus II software version 2.1 no longer supports the Compiler Settings File (.csf) variable, MIGRATION_DEVICES.	In order to specify migration device names in the CSF file, use the DEVICE_MIGRATION_LIST variable. For example: DEVICE_MIGRATION_LIST = "DEVICE_A, DEVICE_B, DEVICE_C" ;

## Platform-Specific Issues

### PC Only

Issue	Workaround
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the <b>stdole32.tlb</b> file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p><b>Windows 98:</b> <i>&lt;CD-ROM drive letter&gt;:\win98\extract.exe /A /L %SystemRoot%\Systembase4.cab stdole32.tlb &lt;Enter&gt;</i></p> <p><b>Windows 98SE:</b> <i>&lt;CD-ROM drive letter&gt;:\extract.exe /A /L %SystemRoot%\Systembase4.cab stdole32.tlb &lt;Enter&gt;</i></p> <p><b>Windows NT:</b> <i>&lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_%SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</i></p> <p><b>Windows 2000:</b> <i>&lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_%SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</i></p> <p><b>Windows XP:</b> <i>&lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_%SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</i></p>

Issue	Workaround
<p>It is possible that one of the Quartus II executable files (<b>quartus.exe</b>, <b>quartus_cmd.exe</b>, <b>quartus_swb.exe</b>, <b>quartus_dbc.exe</b>, <b>quartus_sim.exe</b>, or <b>quartus_cmp.exe</b>) may not terminate properly after an error.</p>	<p>Use the Windows Task Manager to end the process before running the Quartus II software again.</p>
<p>If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.</p>	
<p>If you are running the Quartus II software under the Windows 2000 operating system using a node-locked (single-user) license that is locked to a network interface card number (NIC ID), and are not physically connected to the network, the Quartus II software will not be able to determine your NIC ID and will not allow you to compile a design. This problem also occurs if you are running a FLEXlm license server under the Windows 2000 operating system with a license locked to the NIC ID.</p>	<p>Follow the recommendations given on the following Microsoft Knowledge Base web page:  <a href="http://support.microsoft.com/support/kb/articles/Q239/9/24.asp">http://support.microsoft.com/support/kb/articles/Q239/9/24.asp</a></p>
<p>The Quartus II software will not operate if your computer has multiple active network interface cards (NICs).</p>	<p>If you have more than one NIC, you must deactivate all but one in order to run the Quartus II software.</p>
<p>A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up to date.</p>	<p>To use the Japanese online Help, copy the <b>quartus.chm</b> file from the <b>jhhelp</b> directory of the CD-ROM to your <b>\quartus\bin</b> directory.</p>
<p>If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the <b>\quartus\bin</b> directory.</p>	<p>You must share the <b>quartus</b> directory, not the <b>\quartus\bin</b> directory.</p>

Issue	Workaround
<p>If you are running the ZoneAlarm personal firewall software, you may receive a message saying, “Can't start or continue to run database creator” when you launch the Quartus II software.</p>	<p>The Quartus II software is not compatible with the ZoneAlarm software. The ZoneAlarm software mistakenly determines that the Quartus II software is accessing the Internet when it uses TCP/IP for its inter-process communication. You must disable the ZoneAlarm software to run the Quartus II software.</p>
<p>The Quartus II software installation program does not add the path for the Quartus II software to the PATH statement in your <b>autoexec.bat</b> file when installed under Windows 98.</p>	<p>Add the path for your installed Quartus II software to the PATH statement in your <b>autoexec.bat</b> file manually.</p>
<p>Under some circumstances, the Quartus II software crashes when using the “X” button to close the Print Preview window when a project is open.</p>	<p>Use the button labeled “Close” to close the Print Preview window when you have a project open.</p>
<p>If you disconnect your network connection while the Quartus II software is open, you may receive an error message saying “Can't start or continue to run the db creator”.</p>	<p>Close the Quartus II software before disconnecting the network connection and wait for the “LAN is disconnected” message in the Windows Taskbar before restarting the Quartus II software.</p>
<p>The Quartus II software is not compatible with the MATLAB web server.</p>	<p>Turn off the MATLAB web server in the <b>Services Control Panel</b> (Start menu) before running the Quartus II software.</p>
<p>Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear.</p>	<p>The registry settings controlling the position of the Quartus II windows may have become corrupted. Type the following command at a command prompt:  <code>quartus -reset_desktop &lt;Enter&gt;</code></p>
<p>If you select <b>SignalTap II</b> in the <b>Filter</b> list of the Node Finder and select a bus to add to the SignalTap II File (.stp), the Quartus II software may expand the bus into individual nodes which may be removed during synthesis, resulting in an error.</p>	<p>Delete the nodes and recompile the project. You can select individual nodes in the Node Finder and group them in the SignalTap II window using the <b>Group</b> command (Node menu).</p>

Issue	Workaround
<p>Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the Compiler Settings File (.csf) or if the location assignments are missing. This problem can occur if you change devices, remove some location assignments using the Assignment Organizer or by manually editing the CSF.</p>	<p>If you experience a no-fit or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.</p>

**Solaris, HP-UX & Linux**

Issue	Workaround
<p>The Quartus II Help is not available if you have set either the MWNO_RIT or the MWDONT_XINITTHREAD environment variables before running the Quartus II software.</p>	<p>Remove the variables from your environment and allow the Quartus II software to set these variables automatically, if needed.</p>
<p>If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 X 768.</p>	<p>Reinstall the Exceed software while running at a screen resolution of 1024 X 768. You can then switch back to your normal, higher resolution setting.</p>
<p>Under some circumstances, there may be editor windows listed in the Window menu that you cannot see.</p>	<p>To display the hidden windows, choose <b>Cascade</b> (Window menu).</p>
<p>You cannot launch the AXD Debugger software from within the Quartus II software.</p>	<p>Launch the AXD Debugger software from outside the Quartus II software.</p>
<p>If you use the <b>License Setup</b> tab of the <b>Options</b> dialog box (Tools menu) to enter the location of the license file, the Quartus II software may give an “Unable to Find License” message.</p>	<p>Restart the Quartus II software before compiling your design.</p>

Issue	Workaround
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the <b>Internet Connectivity</b> page of the <b>Options</b> dialog box (Tools menu). If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
The <b>Colors</b> list in the <b>Block &amp; Symbol Editor Color Options Tab</b> of the <b>Options</b> dialog box (Tools menu) or <b>Format Tab</b> of the <b>Properties</b> dialog box (Edit menu) for any object in the Block or Symbol Editors may remain open, and may cause an internal error if you click anywhere else in the Quartus II software before closing the <b>Colors</b> list box.	Select a color to close the <b>Color</b> list box.
The Non-Global High Fan-Out Signals Section (Compilation Report) does not appear in the Compilation Report.	
You cannot run the Innoveda BLAST software automatically from within the Quartus II software, even if the <b>Run this tool automatically after compilation</b> option is turned on.	Run the Innoveda BLAST software manually.
You cannot run the Mentor Graphics® LeonardoSpectrum™ software from within the Quartus II software.	Run the LeonardoSpectrum software manually outside the Quartus II software.
You cannot run the Model Technology™ ModelSim® software from the <b>EDA Tool Post-Compilations Options &gt; Run Simulation Tool</b> command (Processing menu) within the Quartus II software.	Run the ModelSim software outside the Quartus II software.
You can access the Quartus II online Help by typing hh quartus.chm <Return> at a command prompt.	

### Solaris Only

<b>Issue</b>	<b>Workaround</b>
<p>The <b>ARM-Based Excalibur MegaWizard Plug-In</b>, which is available from the <b>MegaWizard Plug-In Manager</b> requires the Java Runtime Environment (JRE) version 1.3, which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for JRE 1.3 to function properly.</p>	<p>Check the web site <a href="http://java.sun.com/j2se/1.3/install-solaris-patches.html">http://java.sun.com/j2se/1.3/install-solaris-patches.html</a> for information about any patches that might be needed.</p>
<p>A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up to date.</p>	<p>To use the Japanese online Help, copy the <b>quartus.chm</b> file from the <b>jhhelp</b> directory of the CD-ROM to your <b>/quartus/solaris</b> directory.</p>
<p>On Solaris versions 2.6 and 2.7, you may receive a core dump or an error message saying “Can’t start quartus_dbc . . .” when first starting the Quartus II software version 2.1.</p>	<p>Contact Altera Customer Applications for a software patch to fix this problem.</p>

### HP-UX Only

<b>Issue</b>	<b>Workaround</b>
<p>If you receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).</p>	<p>Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: <b>/etc/passwd</b> and <b>/etc/group</b>.</p>
<p>Attempting to convert your device SRAM Object Files (<b>.sof</b>) to Programmer Output Files (<b>.pof</b>) for use with a Configuration device, such as an EPC 2, causes the Quartus II software to “hang” when you open the Conversion Setup File (<b>.cof</b>).</p>	<p>Create the POF as usual and add it to your project with the <b>Add Files to Project</b> command (Project menu).</p>

<b>Issue</b>	<b>Workaround</b>
<p>A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up to date.</p>	<p>To use the Japanese online Help, copy the <b>quartus.chm</b> file from the <b>jhhelp</b> directory of the CD-ROM to your <b>/quartus/hp11</b> directory.</p>
<p>While programming an EPC 16 with the Quartus II programmer, the software will “hang” and not respond to any inputs.</p>	<p>Program EPC 16 devices on Windows NT or Solaris-based computers.</p>
<p>Under some circumstances the Quartus II user interface may “hang” and become unresponsive during compilation on HP-UX 10.2.</p>	<p>Kill the existing <code>quartus</code> process and recompile the project using the command-line. You can then use the UI to view the compilation results. This problem occurs due to a problem in HP-UX 10.2 and does not occur when running on HP-UX 11.0.</p>

**Linux Only**

<b>Issue</b>	<b>Workaround</b>
<p>The <b>MegaWizard Plug-In Manager</b> may initially appear very small or the Quartus II software may appear to be frozen when you are accessing the Linux version of the Quartus II software using Xceed and the KDE windows manager.</p>	<p>Replace the Java Runtime Environment (JRE) that is installed automatically with the Quartus II software with the JRE version 1.4, which is available at the following URL:  <b><a href="http://java.sun.com/j2se/1.4/download.html">http://java.sun.com/j2se/1.4/download.html</a></b>            Run the JRE installation script in a temporary directory to unarchive the JRE version 1.4. Then, make a backup copy of your <b>/quartus/linux/jre1.3.1_02</b> directory. Next, copy the contents of the temporary directory to your <b>/quartus/linux/jre1.3.1_02</b> directory, keeping the directory name the same, even though you are using the JRE version 1.4.</p>

<b>Issue</b>	<b>Workaround</b>
<p>A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up to date.</p>	<p>To use the Japanese online Help, copy the <b>quartus.chm</b> file from the <b>jhhelp</b> directory of the CD-ROM to your <b>/quartus/linux</b> directory.</p>
<p>If you attempt to exit from the Quartus II software while the Tutorial window is open, the Tutorial window may remain open and not respond to your commands.</p>	<p>Close the Tutorial window before exiting from the Quartus II software.</p>
<p>If MasterBlaster is not available in the <b>Hardware Settings</b> tab of the <b>Hardware Setup</b> dialog box, but is connected properly, you may not have Read/Write permission for the serial (<code>dev/ttySx</code>) port to which the MasterBlaster is connected.</p>	<p>Have a system administrator assign Read/Write permission for the appropriate port. This change can be accomplished by adding you to the “uucp” group, or by giving Read/Write permission for the serial port to everyone using the following command:  <code>chmod o+rw /dev/ttySx</code>                      where <i>x</i> is the serial port affected.</p>
<p>This release of the Quartus II software supports the MasterBlaster download cable using either Passive Serial or JTAG modes. Although you can generate Jam (<b>.jam</b>) and Jam Byte-Code (<b>.jbc</b>) files, these files are not supported for device configuration on Red Hat Linux version 7.1. Additionally, EPC4, EPC8, and EPC16 configuration devices are not supported at this time, and programming times of EPC 2 devices may be extremely slow.</p>	<p>For information about using a ByteBlasterMV with the Quartus II software on the Linux operating system, contact Altera Customer Applications.</p>

## Device Family

### *Mercury*

Issue	Workaround
If your Quartus II version 1.0 or 1.1 design for a Mercury device uses the <code>altlvds_tx</code> or <code>altlvds_rx</code> megafunction, and you archived the design, you may have functional problems in your design, including inverted signals.	Delete the <code>altlvds_tx</code> or <code>altlvds_rx</code> megafunction from the design and replace it with the version included with the Quartus II software version 2.1 before compiling your design in the Quartus II software version 2.1.

### *Excalibur*

Issue	Workaround
You may receive the message “System Build Descriptor File missing parameter <code>programming_clock_frequency</code> ” for Software Build Descriptor ( <code>.sbd</code> ) files generated in the Quartus II software version 2.0 and earlier, after selecting the <b>Boot from Serial</b> option in the Excalibur MegaWizard.	Rerun the Excalibur MegaWizard in the Quartus II software version 2.1 to regenerate the SBD file and correct the error.

## Design Flow

### *LogicLock*

Issue	Workaround
The LogicLock regions window may not get refreshed when making a LogicLock assignment such as performing an Import operation.	To see new assignments, you may need to exit from the Quartus II software then re-launch the Quartus II software.
LogicLock Resources estimation in the Compilation Report is misleading for Stratix devices due to memory or DSP blocks that may be completely or partially within a LogicLock region.	Only LE resources are reported and are based on the origin of the LogicLock region since the resources available in a rectangular area of a Stratix device depends on the origin of the region.

### Verification

Issue	Workaround
Node names for module outputs that are directly connected to inferred objects (counters, etc.) cannot be added to a SignalTap II (.stp) file.	To add such node names to an STP file, you should first assign those names to a signal bus and then add the bus to the STP file.
The data displayed in the SignalTap II waveform display is not correct under some circumstances.	The correct data is captured, but is not displayed unless the SignalTap II (.stp) file is closed and reopened after acquisition. A software patch is available from the Altera Customer Applications department.

### Native RTL Synthesis (VHDL and Verilog HDL)

Issue	Workaround
The Verilog and VHDL extractors now support the <code>translate_off</code> and <code>translate_on</code> pragmas. Some designs relied on the behavior of the Quartus II software version 2.1 (which ignores them). A common case is where you have a MegaWizard-generated VHDL or Verilog HDL megafunction and have added <code>translate_off</code> and <code>translate_on</code> pragmas to hide the internal details from your 3rd party synthesis tool. The details will also be hidden from the Quartus II software also, and as a result the megafunctions will not be implemented when you compile using version 2.1 of the Quartus II software.	

Issue	Workaround
<p>Some designs that compiled successfully using the Quartus II software version 2.0 may not compile successfully using the Quartus II software version 2.1. Common issues are:</p> <ul style="list-style-type: none"> <li>• Assigning to a single register in multiple Always Constructs or Process Constructs; the Quartus II software version 2.1 will give a multiply-driven signal error</li> <li>• Width mismatches in VHDL that were not caught in the Quartus II software version 2.0</li> <li>• Referring to another generic within a generic list in VHDL, for example having generic WIDTH and generic DATA ( WIDTH downto 0 ). This feature is not officially supported in VHDL, but it is supported in many tools including the Quartus II software version 2.0. It is not supported in the Quartus II software version 2.1.</li> </ul>	
<p>If you have an IP core in VHDL or Verilog HDL and your license is not set up correctly, you will get a “Can’t open design file” error.</p>	
<p>The Quartus II software version 2.1 connects all nets driven by GND together, and all nets driven by VCC together. This can cause confusing error messages, as an electrical conflict on one GND net may be reported on any GND net, not necessarily the one which is actually causing the problem.</p>	
<p>When you instantiate a non-Verilog HDL module from a Verilog HDL design file, you must use named parameter value assignments to set parameter values.</p>	<p>Altera recommends using a Defparam Statement to set parameter values. Ordered parameters will be ignored when instantiating non-Verilog HDL modules from a Verilog HDL design.</p>

Issue	Workaround
<p>The Quartus II software version 2.1 will give an error when you try to shift or rotate a bit vector by more than the number of bits in the vector. For example, shifting a 32-bit register by 33 bits will cause an error.</p>	<p>You can work around this problem by truncating or taking the modulus of the shift distance as appropriate before doing the shift or rotate.</p>
<p>The Quartus II software assumes that parameters/generics on modules should be inherited. If a parent module has the parameter PARAM and a value of 1 and a child module has a parameter PARAM without an explicit value, the value 1 will be inherited and will override the default value. This behavior is by design and is consistent with previous versions of the Quartus II software, but is not compliant with the VHDL and Verilog HDL language standards.</p>	
<p>The Quartus II software crashes with an Internal Error when a VHDL or Verilog HDL entity instantiates another lower-level entity with a similar name. For example if a VHDL entity top has a generic integer whose value is 1, and the entity top instantiates a component named top_1, this will cause an Internal Error. One example of this crash occurs with the Turbo Encoder/Decoder MegaCore in decoder mode.</p>	<p>In the case of the Turbo Decoder, the workaround is to instantiate the auktd_umts_turbo_decoder_5_4_4_0 function directly rather than instantiating it via the <b>auktd_umts_turbo_decoder.vhd</b> file. You can inspect the plain-text VHDL file in the <b>/MegaCore/turbo_codec/lib</b> directory to see how this is done. For general user code, change the name of the instantiated entity such that it does not match the <code>&lt;top_level_entity_name&gt;_&lt;param1&gt;_&lt;param2&gt;...</code> format.</p>

### Verilog HDL Integrated Synthesis

Issue	Workaround
<p>Verilog-2001 mode is enabled by default. This can cause some issues with Verilog-1995 designs, most commonly due to new reserved words in Verilog-2001 such as <code>config</code>.</p>	<p>Do not use reserved words as identifiers.</p>
<p>If more than one copy of a module is instantiated, the first instantiation will set the maximum port widths. In other words, if you have</p> <pre>wire [3:0]a; wire [7:0]b;  mod my_inst_1(a); mod my_inst_2(b);</pre> <p>the port of <code>my_inst_2</code> will be clipped to 4 bits wide. A warning message is issued.</p>	<p>Move <code>my_inst_2</code> above <code>my_inst_1</code>.</p>
<p>The Quartus II version 2.1 software does not recognize Verilog HDL state machines. Instead it synthesizes them as generic logic. The Compiler does not report state information and you cannot control the encoding using Quartus II logic options.</p>	<p>A future version of the Quartus II software will recognize Verilog HDL state machines and optimize them to deliver improved performance.</p>
<p>The Quartus II software version 2.1 looks for files in an <code>'include</code> compiler directive in the project root directory. If there is a path specified, it is taken as being relative to the project root directory.</p>	
<p>A function call in a vector range specification causes an Internal Error.</p>	

Issue	Workaround
<p>The Quartus II software version 2.1 does not correctly parse a Defparam Statement that contains a space between the module name and the parameter name. The following example:</p> <pre>foo inst(a,b,c)   defparam inst . param = 1;</pre> <p>gives the error “variable name inst is already defined.”</p>	<p>Remove the space between <code>inst</code> and the period and the design compiles correctly.</p>
<p>Wired net types are incorrectly treated as regular nets. The following design should be legal and result in <code>wired_or_net</code> equaling 1</p> <pre>wor wired_or_net; assign wired_or_net=1;   assign wired_or_net=0;</pre> <p>However, the Quartus II software version 2.1 treats <code>wired_or_net</code> as a regular wire and issues a warning that the net is driven by multiple drivers. This problem also applies to WIRED AND nets.</p>	
<p>Verilog HDL escaped names that look like vectors can cause problems in the Quartus II software. For example, if you have a single bit component port named <code>\my_vector_port[3:0]</code>, the Quartus II software version 2.1 will treat it as an array port.</p>	<p>You should avoid using such port names in the Quartus II software version 2.1.</p>
<p>In a case statement, if you specify a <code>full_case</code> pragma and a default clause, the Quartus II software version 2.1 will ignore the default case. This is different behavior from some other tools which will not ignore the default case.</p>	

Issue	Workaround
<p>The Quartus II software version 2.1 does not allow two parameter value overrides (Defparam Statements) for a parameter. This behavior is different from the IEEE Std. 1364-2001 <i>IEEE Standard Verilog Hardware Description Language</i> manual, in which the last Defparam Statement is used if there are multiple Defparam Statements.</p>	
<p>The Quartus II software version 2.1 does not give an error for a Defparam Statement for a parameter that does not exist in the named module, or for a parameter value assignment with more unnamed parameters than are defined in the module.</p>	
<p>If you use the following statement:  <code>// synthesis Translate_off</code>  followed by <code>/* synthesis translate_on */</code> you will get a syntax error.</p>	<p>Replace <code>/* synthesis translate_on */</code> with <code>//synthesis translate_on.</code></p>
<p>If the last line of your Verilog file is a <code>'define</code> compiler directive and there is no carriage return at the end of the line, the Quartus II software version 2.1 gives a syntax error.</p>	<p>Add a carriage return at the end of the line to avoid receiving the syntax error message.</p>
<p>Recursive Verilog HDL functions or modules, such as a module that instantiates itself, cause the Quartus II software version 2.1 Compiler to crash.</p>	

Issue	Workaround
<p>The Verilog HDL reader in the 2.1 version of the Quartus II software does not differentiate internally between bit vectors and strings. This is compliant with the IEEE Std. 1364-2001 <i>IEEE Standard Verilog Hardware Description Language</i> manual, but can cause problems in mixed-language designs, such as commonly occur when instantiating MegaCore<sup>®</sup> functions. When evaluating parameters from a Verilog HDL module, the Quartus II software version 2.1 will write a bit vector as a string if its size is a multiple of 8 bits and if each 8-bit value represents a valid ASCII character. For example, the value:</p> <pre>defparam inst.p =     16'h4849;</pre> <p>will be passed to module <code>inst</code> as the string "HI".</p> <p>This problem occurs with the PCI Compiler MegaCore function when a Verilog HDL wrapper is generated using the <b>MegaWizard Plug-In Manager</b> (Tools menu).</p>	<p>If you are instantiating the PCI Compiler MegaCore function, you should re-generate the core wrapper and choose to output an AHDL or VHDL version to use in your project instead of the Verilog HDL version. If the bit vector is less than 32 bits wide, you can replace it with an integer, which is not subject to the same problem. For the example, you would replace the value <code>16'h4849</code> with the integer equivalent:</p> <pre>defparam inst.p = 18505;</pre>

### VHDL Integrated Synthesis

Issue	Workaround
The Quartus II software version 2.1 does not synthesize <code>a &lt; b</code> for user-defined enums	
<p>The Quartus II software version 2.1 does not support ranges in case statements on an enum. For example:</p> <pre> type state_type is (st_a,   st_b, st_c, st_d, st_e);    case cur_st is     ...     when st_b to st_d =&gt;       next_st &lt;= st_e;     ... </pre>	
Support for configurations is limited. You can choose the architecture for an entity in simple cases, but complicated configuration specifications with a variety of entities bound under different conditions will not work correctly.	

### EDA Integration

Issue	Workaround
The <b>220model.vhd</b> simulation library, located in the <code>\&lt;Quartus II directory&gt;\eda\sim_lib</code> directory, contains VHDL 87-compliant models.	For a VHDL 93-compliant simulation model library, you can download an updated version of this simulation model library from the Altera web site, at <a href="http://www.altera.com">http://www.altera.com</a> .
This version of the Quartus II software does not support the Amplify Physical Optimization software, even though you can select it in the <b>EDA Tool Settings</b> dialog box.	Do not select the Amplify Physical Synthesis Optimization software in the <b>EDA Tool Settings</b> dialog box.

Issue	Workaround
The directory containing the ARM-based Excalibur stripe models changed in version 2.0 of the Quartus II software. This change may cause compilation scripts to fail.	Edit your compilation scripts so that the models and simulation wrapper files are located in the following directory: <b>quartus\eda\sim_lib\ excalibur\ stripe_model_&lt;operating system&gt; \ModelGen\models\epxa&lt;1 / 4 / 10&gt;\r0\&lt;simulator_language&gt;</b>

## Customer Service Requests Resolved

Customer Service Requests resolved in this version of the Quartus II software include, but are not limited to, the following Service Request ID numbers:

Service Request ID	Description
10252399	Quartus II MegaWizard Plug-In Manager error when creating Verilog HDL wrapper around 3rd party synthesis IP core
10251195	Cell delay for register in column IOE is almost 1.4ns more then row IOE in EP2A70 devices
10249789	The Quartus II software does not report that a .mif file has changed when compiling with smart compilation turned on
10249699	Customer design specific functional simulation does not match timing simulation in ModelSim
10248053	JAM file from the Quartus II software version 2.0 SP2 gives Device #4 unable to read IDCODE
10247815	Customer design-specific timing Issues with EP2A15F672C8
10246775	Checksum is 00000000 when reading an EPC1 POF in the Quartus II software
10246579	altsyncram in altera_mf.vhd and altera_mf_components.vhd doesn't match generics (mixed_port_feed_through_mode)
10246339	Timing Tco discrepency between Quartus II 1.1 to 2.1 - push button w/ no settings
10246273	The QuartusII software version 2.0 is reporting CLKLK_ENA (P16) as VCCINT
10246105	Customer design specific sof to pof conversion problem
10245705	.vo file does not contain BIDIR bus when "Generate Power Input File" option is chosen
10243595	Customer design specific tco differences between versions 2.0 and 2.0 SP1/SP2 for EPM 7512B
10243149	Customer design specific functional simulation issue for altsyncram in Stratix; timing simulation is correct
10242383	Megafunction ALTQPRAM : when used as ROM "width_write_a" is NOT set but necessary for simulation.
10241597	Output phase shift for core clock is incorrect in RTL simulation of Stratix PLL.
10241069	Customer design specific LVDS timing simulation for Stratix does not match timing diagram in AN202

Service Request ID	Description
10239049	Customer design generating wrong .VHO but .VO is correct
10238505	Incorrect HDL (Verilog) conversion from BDF file for customer-specific design
10238143	ALTPLL: External feedback issue
10237615	altquadport functional simulation issue
10237479	ALTSYNCRAM - MegaWizard should have 2Kx2 and 4Kx1 options for M4K blocks
10237147	Fitting issue when Auto Global Register option set to "ON"
10236965	Flexible LVDS pins are not available as SignalProbe pins in APEX II devices
10236911	Clock skew / data delay issue in ACEX 1K device
10236351	Customer design-specific AHDL State Machine simulation issue
10235677	The Quartus II software gives an "illegal location assignment" error if imported MAX+PLUS II acf file contains lower-case text assignment
10235509	Calculating offsets with derived clocks in the Quartus II software
10235341	Floorplan does not show logical fan-in, fan-out or equations for pin and IOE's for Stratix device
10234913	Issue with assigning LVCMOS input pins on the side of the device
10233793	Customer design fitting issue when "Auto Packed Registers" is turned on
10232381	Signed multiplication issue when using modelsim and altera_mf.vhd file for altmult_add (Stratix device).
10232291	Verification of EPC 16 issue when using the MasterBlaster USB port (and serial port)
10231657	Programming issue with MasterBlaster(COM1) in the Quartus II software version 2.0 SP1 on Windows NT version 4.0.
10231601	QOR issue when comparing EPF10K130E design compiled on the Quartus II and MAX+PLUS II software
10231213	Global Signal assignment issue
10231185	Updating schematic block I/Os deletes logic in block
10230351	The Quartus II software adds an extra macrocell for my output enables and gives warning - Macrocell buffer inserted after node
10229905	tx_outclock frequency discrepancy for Stratix LVDS functional simulation in Modelsim
10229213	Non-differential I/O standard pins assignment issue
10228887	Solaris error: Can't export LogicLock region assignments before performing analysis and elaboration
10228735	32 x 8k Stratix FIFO fitting issue
10227709	Hierarchical Register packing issue
10226173	Global Signal assignment issue
10224357	LPM_BUSTRI implementation issue
10224017	ClockLock PLL Input frequency issue when using LVDS I/O
10223799	Customer design specific compile error in 2.1
10223767	Fast Regional clock assignment issue
10223359	APEX II - Timing simulation issue with Quartus II software version 2.0 and in ModelSim 5.5e
10223219	ModelSim 5.5E: altera_mf.v ddio_output functional simulation issue
10223025	ALTCDR megafunction VHDL file TX and RX issue
10221891	Quartus II MegaWizard Plug-In Manager issue when using the Cancel button on Solaris

Service Request ID	Description
10220981	Fitting issue with back-annotation for Mercury EP1M350
10217707	Tsu issue with EP2A70
10217707	Peripheral bus issue
10217387	Simulation reports setup time violation on register that can't be found in design
10217273	Derived clock issue in the Quartus II software version 2.0 for MAX 7000AE devices
10217257	Customer-specific design hangs in the fitter
10216809	LVDS fitting issue
10215709	APEX II issue: Node <name> must be a Register node / Output pin has no fan-in
10215709	APEX II: Issue with Tco comparison between the Quartus II software and Modelsim simulation
10213761	AHDL design issue when one subdesign is combined with another subdesign
10213521	Stratix: FIFO issue with M-RAM blocks
10212791	LogicLock issue
10210035	TAN reporting issue
10208471	Issue with .vhd file generated by the Quartus II software version 2.0 for LPM megafunction when lpm_svalue parameter is being used.
10207941	Fitting issue for Mercury: I/O standard LVDS or LVPECL assigned to pin lvds_txclk(n)
10207273	Message location issue when locating setup time violations
10207217	Can't reserve pin <pin name> because it lacks a location assignment
10205009	Fixed LogicLock Region fitting issue with simple fifo
10204069	Fitting issue with Stratix device auto select
10201825	Synplify EDIF pin assignment issue
10194691	Synplify issue with .vqm designator in .quartus file
10192495	Txoutclk2p pin/port issue when you use this pin as normal I/O in APEX II (EP2A25)
10192059	Quartus II software version 2.0 and MAX 7000B IO bank voltage issue
10190615	Quartus II software version 2.0 - Issue with pins outs for EP1K100FC256 - comparing the Quartus II software with the MAX+PLUS II software and Web pin-outs
10189379	for statment contains illegal variable or step assignment
10188853	Simulation issue with FLEX 10KE model in ModelSim
10188137	SXT VHDL function issue
10183901	LVDS TX Timing issue for APEX 20K 1500E design
10182479	Verilog HDL issue: Non-constant bit-/part-select index
10178095	Fitter issue with design with 4 PLLs
10160895	APEX II - Fitting issue when migrating from EP2A25B724 to EP2A70B724 due to lack of Vref
10153767	'x' bits in fixed datab of LPM_COMPARE are not synthesized properly
10150315	Project gets no fit in Quartus after adding pin assignments, tco and tsu constraints (VHDX issue)
10147265	Simulation issue with a 2-dimensional array
10146533	Flex 10KE project compilation issue
10133861	Error "BIDIR pin bidir[2] does not have a source" when run through Synplify

<b>Customer design specific Internal Errors</b>
10251031, 10250835, 10250807, 10249971, 10248577, 10248361, 10247997, 10251031, 10247701, 10247477, 10247445, 10246731, 10246239, 10246053, 10245899, 10245661, 10244069, 10243023, 10242663, 10241787, 10240761, 10240719, 10238555, 10234579, 10234559, 10234043, 10232979, 10232405, 10232305, 10231835, 10228735, 10228735, 10228409, 10228351, 10227819, 10227471, 10227171, 10225469, 10224119, 10223045, 10222707, 10222467, 10222113, 10220799, 10220799, 10220605, 10220171, 10220073, 10219065, 10217565, 10217545, 10217273, 10216477, 10215701, 10215361, 10214923, 10214749, 10214391, 10214373, 10213371, 10212671, 10212057, 10211909, 10211757, 10210131, 10209317, 10209033, 10205673, 10199693, 10199299, 10196689, 10190231, 10185777, 10183143, 10181959, 10179365, 10179151, 10177809, 10176167, 10175929, 10173109, 10172987, 10171571, 10167197, 10166961, 10166141, 10162523, 10161015, 10151505, 10130231, 10125351, 10120874, 10119615, 10109289, 10093903, 10075559, 10069269, 10067917, 10064235, 10054933, 10050089, 10049901, 10032095, 10022126, 10013854, 10009837, 10006565, 10004496, 2661470

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