



Quartus II Software Release Notes

September 2002

Quartus II version 2.1 Including Service Pack 1

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **quartus** directory.

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New Features & Enhancements

Quartus II software version 2.1 including Service Pack 1 contains advanced compilation and simulation support for the new Cyclone™ FPGA family—the lowest cost FPGA ever. Also included in this release are programming support for Stratix™ EP1S10ES devices, advanced compilation and simulation support for Stratix EP1S10 and EP1S20 devices in the 484-pin FineLine BGA™ package, updated Stratix timing models, and several software enhancements.

Device Support & Pin-Out Status

Full Device Support

Full compilation, simulation, timing analysis, and programming support are now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Stratix	EP1S10ES F780 EP1S10ES F672	EP1S10ES B672

Advance Device Support

Compilation, simulation, and timing analysis support are provided for the following devices that will be released in the near future. Although pin-out information is generated by the Compiler, programming files are not generated for these devices in this release.

Devices with Advance Support

Device Family	Devices	
Cyclone	EP1C3 T100 EP1C6 T144 EP1C12 Q240 EP1C20 F324	EP1C3 T144 EP1C6 Q240 EP1C12 F324 EP1C20 F400

Initial Information Support

Compilation, simulation, and timing analysis support are provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Devices with Initial Information Support

Device Family	Devices
None	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	Notes
Stratix	EP1S10	The Quartus II software version 2.1 includes preliminary timing models for -5, -6, and -7 speed grades for the Stratix device family.
	EP1S20	
	EP1S25	
	EP1S30	
	EP1S40	
	EP1S60	
	EP1S80	

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
APEX™ II	EP2A15	2.1
	EP2A25	2.1
	EP2A40	2.1
	EP2A70	2.1
APEX™ 20KC	EP20K200C	
	EP20K400C	2.0
	EP20K600C	2.0
	EP20K1000C	
Excalibur™	EPXA1	2.0 SP1
	EPXA4	2.0 SP1
	EPXA10	2.0 SP1
Mercury™	EP1M350 (copper)	2.0
	EP1M120 (aluminum)	
	EP1M120 (copper)	
MAX™ 7000	EPM7032AE	2.0
	EPM7064AE	2.0
	EPM7128AE	2.0
	EPM7256AE	2.0
	EPM7512AE	2.0
	EPM7032B	2.0
	EPM7064B	2.0
	EPM7128B	2.0
	EPM7256B	2.0
	EPM7512B	2.1 SP1
MAX 3000	EPM3032A	2.0
	EPM3064A	2.0
	EPM3128A	2.0
	EPM3256A	2.0
	EPM3512A	2.1 SP1

The current version of the Quartus II software also includes final timing models for the, ACEX® 1K, APEX 20KE, FLEX® 6000, and the FLEX 10K device families. Final timing models for these device families became final in versions earlier than version 2.0.

EDA Interface Information

The Quartus II software version 2.1 including Service Pack 1 supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink support
Mentor Graphics® LeonardoSpectrum™-Altera	2002d	✓
Mentor Graphics® LeonardoSpectrum™	2002d	✓
Synopsys Design Compiler	2001.08	
Synopsys FPGA Compiler II	3.7	✓
Synplicity® Synplify® and Synplify Pro®	7.1A	✓
Aplus Design Technologies (ADT) PALACE™	2.1	✓
Verification Tools	Version	NativeLink support
Cadence NC-Verilog	3.3	✓
Cadence NC-VHDL	3.3	✓
Cadence Verilog-XL	3.3	
Model Technology™ ModelSim®	5.6a	✓
Model Technology ModelSim-Altera	5.6a	✓
Innoveda BLAST	1.2.2	
Synopsys PrimeTime	2000.05	✓
Synopsys Scirocco	2000.12	✓
Synopsys VSS	2000.05	
Synopsys VCS	6.0	
Mentor Graphics Tau	2.2	
Verplex Conformal LEC	3.1.0a	

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
<p>Versions of the Quartus II software earlier than version 2.0 cannot open Block Design Files (.bdf) created with the Quartus II software version 2.0 and later.</p>	
<p>Within each device family, not all speed grades of a given device share the same features.</p>	<p>Refer to the Altera data sheet for the device family for further information.</p>
<p>The Power-Up Don't Care logic option default condition has been changed to On in the Quartus II version 2.1 Service Pack 1 software release.</p>	
<p>There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.</p>	<p>Connect the port to a top-level bidirectional pin or to other logic in the design.</p>
<p>To use the EP20K400GC655 device in your design, please contact the Altera Customer Applications Department.</p>	
<p>Registers that feed output pins will have the same name as the output pin when you view the post-fitting register names.</p>	

Issue	Workaround
<p>If you have a version of the Quartus® software previous to the Quartus II software version 1.0 installed on your computer in addition to the Quartus II software, you can start the previous version of the program only by running the runq.exe program from the \quartus\bin directory that contains the previous version you wish to use.</p>	
<p>If you compile a design with the Run batch simulation option turned on and, once compilation has completed, click any simulation waveform in the Simulation Report window and then choose Simulate Mode (Processing menu), an error may occur.</p>	<p>Close the Simulation Report window before changing to Simulate mode.</p>
<p>The PowerFit™ Fitter supports assignments to LAB cliques only. Back-annotating a design containing assignments to other types of cliques may create illegal assignments that result in a “no fit.”</p>	<p>Remove all assignments to cliques before recompiling a back-annotated design.</p>
<p>You should not create multiple Compiler settings that have the same design entity as the “compilation focus.”</p>	
<p>The command-line version of the Quartus II software does not accept a path name as part of the project name.</p>	<p>Run the Quartus II software from the directory where your project is stored.</p>
<p>Under some circumstances, if the Optimize I/O cell register placement for timing option in the Compiler Settings dialog box (Processing menu) is turned on and you are using multiple peripheral clock enable signals, you may receive an error message or the Quartus II software may crash.</p>	<p>Set the Clock Enable Routing logic option to Single-Pin for some of the clock enable signals.</p>

Issue	Workaround
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, choose Index from the Help menu and type the name of the item.
<p>The Quartus II software provides limited support for the following I/O standards for APEX 20KE devices that are not available with the I/O Standard logic option:</p> <ul style="list-style-type: none"> • LVPECL is a differential I/O standard similar to LVDS. APEX 20KE devices can support LVPECL I/O pins by using the I/O pins in LVDS mode with an external resistor network. • PCI-X is an enhanced version of the PCI I/O standard that can support a higher average bandwidth. This standard has more stringent requirements than PCI. 	<p>To use the LVPECL I/O standard in APEX 20KE devices in the Quartus II software, set the I/O Standard logic option for the pins to LVDS and connect the pins to an appropriate external resistor network.</p> <p>The APEX 20KE I/O drivers meet the requirements for PCI-X. Turn on the PCI I/O logic option to support PCI-X requirements, including the overshoot clamp.</p>
You cannot locate an error in a design file if compilation was unsuccessful due to a syntax error.	
If you open a project that was created using a previous version of the Quartus II software, you may receive a message that indicates that the database is incompatible and that results of the last compilation will be lost.	Back-annotate all of the project assignments in the previous version. Then, delete the <code>\<project name>\db</code> directory and all of its contents.
The Timing Analyzer does not recognize non-PLL clock signals when using the <code>altclklock</code> megafunction.	Make Clock Settings assignments to all non-PLL clocks.
If you are using the <code>lpm_mult</code> megafunction, you must turn off the Auto Cascade Chains option when editing project defaults in the Parameters tab of the Option & Parameter Settings dialog box (Project menu).	

Issue	Workaround
The Waveform editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the Group command (Edit menu) to create groups of arbitrary nodes.
Using the Cancel button in the Assignment Organizer when multiple nodes have been selected causes the Quartus II software to restore the setting(s) of the first node to all the nodes that were edited.	Do not use the Cancel button to cancel changes made to two or more selected nodes that have assignments of differing settings.
If you are using the <code>altcam</code> , <code>altclklock</code> , <code>altlvds_rx</code> , or <code>altlvds_tx</code> megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Last Compilation floorplan.
The Quartus II software does not support file names with more than one extension. For example, you cannot use the file name file.eda.edif .	Use file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files also on the network.	Altera recommends using versions 1.9.16p11 and 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (<code>debug[7..0]</code>), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying “Unsupported data type in the top-level module.”	Reserve the pins using single name notation (e.g., <code>debug7</code> , <code>debug6</code> , and so on).
The Quartus II software versions 2.1 and later support only versions 5.2 and later of the Altera PowerKit™ software. Previous versions of the PowerKit software are not supported with these versions of the Quartus II software.	

Issue	Workaround
Under some circumstances, an error message saying “Can’t start server. Beginning attempt 1/3...” appears when starting a compilation, simulation, or software build.	Increase the value of the environment variable <code>QUARTUS_PROCESS_TIMEOUT</code> from the default value of 100. If the environment variable does not exist, set it to an initial value of 200. You may have to increase the value until you no longer receive the error message.
If you are using the HSTL Class II I/O standard with an APEX II device, additional information is required.	Contact the Altera Customer Applications department at apexii@altera.com for information about Service Packs and device pin-outs.
In the Package view in the Floorplan Editor, all <code>GND_IO</code> pins for APEX 20K, APEX 20KE, and APEX II devices are incorrectly shown as being in Bank 9.	Ignore the I/O bank information; the <code>GND_IO</code> pins are not associated with any I/O bank.
Do not change the file permissions (such as changing read-only to read and write) of Quartus II settings and configurations files (<code>.csf</code> , <code>.esf</code> , etc.) while a Quartus II project is open.	Close your Quartus II project before making changes to the file permissions.
The order of ports for the ARM[®]-based Excalibur MegaWizard[™] - generated symbol for the stripe changed in version 2.0 of the Quartus II software. If you re-run the MegaWizard for a design created in a version of the Quartus II software earlier than version 2.0, you will receive port connection errors when you compile the design.	To avoid receiving these errors, adjust the port connections in the BDF after updating the symbol.
Node names containing numbers greater than $2^{31}-1$ (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Output File (<code>.pof</code>) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.

Issue	Workaround
<p>The Quartus II software versions 2.1 and later no longer support the Compiler Settings File (.csf) variable, MIGRATION_DEVICES.</p>	<p>In order to specify migration device names in the CSF, use the DEVICE_MIGRATION_LIST variable. For example: DEVICE_MIGRATION_LIST = "DEVICE_A, DEVICE_B, DEVICE_C" ;</p>
<p>Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the CSF or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the Assignment Organizer or by manually editing the CSF.</p>	<p>If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.</p>
<p>If you select SignalTap II in the Filter list of the Node Finder and select a bus to add to the SignalTap® II File (.stp), the Quartus II software may expand the bus into individual nodes that may be removed during synthesis, resulting in an error.</p>	<p>Delete the nodes and recompile the project. You can select individual nodes in the Node Finder and group them in the SignalTap II window using the Group command (Node menu).</p>
<p>After register duplication has occurred, the duplicated register has a unique name in the form <original name>~<suffix>. The new register name may not properly inherit timing assignments made with wild cards.</p>	<p>Make sure that duplicated register names are included in your wild card match when making timing assignments.</p>

Platform-Specific Issues

PC Only

Issue	Workaround
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the stdole32.tlb file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p>Windows 98: <i><CD-ROM drive letter></i>:\win98\extract.exe /A /L %SystemRoot%\Systembase4.cab stdole32.tlb <Enter></p> <p>Windows 98SE: <i><CD-ROM drive letter></i>:\extract.exe /A /L %SystemRoot%\Systembase4.cab stdole32.tlb <Enter></p> <p>Windows NT: <i><CD-ROM drive letter></i>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows 2000: <i><CD-ROM drive letter></i>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows XP: <i><CD-ROM drive letter></i>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p>

Issue	Workaround
<p>It is possible that one of the Quartus II executable files (quartus.exe, quartus_cmd.exe, quartus_swb.exe, quartus_dbc.exe, quartus_sim.exe, or quartus_cmp.exe) may not terminate properly after an error.</p>	<p>Use the Windows Task Manager to end the process before running the Quartus II software again.</p>
<p>If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.</p>	<p>Limit the full, hierarchical instance name to fewer than 247 characters if possible.</p>
<p>If you are running the Quartus II software under the Windows 2000 operating system using a node-locked (single-user) license that is locked to a network interface card number (NIC ID), and are not physically connected to the network, the Quartus II software will not be able to determine your NIC ID and will not allow you to compile a design. This problem also occurs if you are running a FLEXlm license server under the Windows 2000 operating system with a license locked to the NIC ID.</p>	<p>Follow the recommendations given on the following Microsoft Knowledge Base web page: http://support.microsoft.com/support/kb/articles/Q239/9/24.asp</p>
<p>The Quartus II software will not operate if your computer has multiple active network interface cards (NICs).</p>	<p>If you have more than one NIC, you must deactivate all but one in order to run the Quartus II software.</p>
<p>A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.</p>	<p>To use the Japanese online Help, copy the quartus.chm file from the jhhelp directory of the CD-ROM to your \quartus\bin directory.</p>
<p>If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the \quartus\bin directory.</p>	<p>You must share the quartus directory, not the \quartus\bin directory.</p>

Issue	Workaround
<p>If you are running the ZoneAlarm personal firewall software, you may receive a message saying, “Can't start or continue to run database creator” when you launch the Quartus II software.</p>	<p>The Quartus II software is not compatible with the ZoneAlarm software. The ZoneAlarm software mistakenly determines that the Quartus II software is accessing the Internet when it uses TCP/IP for its inter-process communication. You must disable the ZoneAlarm software to run the Quartus II software.</p>
<p>The Quartus II software installation program does not add the path for the Quartus II software to the PATH statement in your autoexec.bat file when installed under Windows 98.</p>	<p>Add the path for your installed Quartus II software to the PATH statement in your autoexec.bat file manually.</p>
<p>Under some circumstances, the Quartus II software crashes when using the “X” button to close the Print Preview window if a project is open.</p>	<p>Use the button labeled “Close” to close the Print Preview window if you have a project open.</p>
<p>If you disconnect your network connection while the Quartus II software is open, you may receive an error message saying “Can't start or continue to run the db creator”.</p>	<p>Close the Quartus II software before disconnecting the network connection and wait for the “LAN is disconnected” message in the Windows Taskbar before restarting the Quartus II software.</p>
<p>The Quartus II software is not compatible with the MATLAB web server.</p>	<p>Turn off the MATLAB web server in the Services Control Panel (Start menu) before running the Quartus II software.</p>
<p>Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear.</p>	<p>The registry settings controlling the position of the Quartus II windows may have become corrupted. Type the following command at a command prompt: <code>quartus -reset_desktop <Enter></code></p>
<p>Path names longer than 229 characters can cause an internal error in the Quartus II software.</p>	<p>Make sure that all path names do not exceed 229 characters.</p>

Solaris, HP-UX & Linux

Issue	Workaround
<p>The Quartus II Help is not available if you have set either the MWNO_RIT or the MWDONT_XINITTHREAD environment variables before running the Quartus II software.</p>	<p>Remove the variables from your environment and allow the Quartus II software to set these variables automatically, if needed.</p>
<p>If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.</p>	<p>Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.</p>
<p>Under some circumstances, there may be editor windows listed in the Window menu that you cannot see.</p>	<p>To display the hidden windows, choose Cascade (Window menu).</p>
<p>You cannot launch the AXD Debugger software from within the Quartus II software.</p>	<p>Launch the AXD Debugger software from outside the Quartus II software.</p>
<p>If you use the License Setup tab of the Options dialog box (Tools menu) to enter the location of the license file, the Quartus II software may give an “Unable to Find License” message.</p>	<p>Restart the Quartus II software before compiling your design.</p>
<p>Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.</p>	<p>Specify the full path to your web browser software on the Internet Connectivity page of the Options dialog box (Tools menu). If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.</p>

Issue	Workaround
<p>The Colors list in the Block & Symbol Editor Color Options Tab of the Options dialog box (Tools menu) or Format Tab of the Properties dialog box (Edit menu) for any object in the Block or Symbol Editors may remain open, and may cause an internal error if you click anywhere else in the Quartus II software before closing the Colors list box.</p>	<p>Select a color to close the Color list box.</p>
<p>The Non-Global High Fan-Out Signals Section (Compilation Report) does not appear in the Compilation Report.</p>	
<p>You cannot run the Innoveda BLAST software automatically from within the Quartus II software, even if the Run this tool automatically after compilation option is turned on.</p>	<p>Run the Innoveda BLAST software manually outside the Quartus II software.</p>
<p>You cannot run the Mentor Graphics LeonardoSpectrum software from within the Quartus II software even if the Run this tool automatically after compilation option is turned on.</p>	<p>Run the LeonardoSpectrum software manually outside the Quartus II software.</p>
<p>You cannot run the Model Technology ModelSim software from the EDA Tool Post-Compilations Options > Run Simulation Tool command (Processing menu) from within the Quartus II software.</p>	<p>Run the ModelSim software outside the Quartus II software.</p>
<p>You can access the Quartus II online Help by typing <code>hh quartus.chm <Return></code> at a command prompt.</p>	

Solaris Only

Issue	Workaround
<p>The ARM-Based Excalibur MegaWizard Plug-In, which is available from the MegaWizard Plug-In Manager requires the Java Runtime Environment (JRE) version 1.3, which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for JRE 1.3 to function properly.</p>	<p>Check the web site http://java.sun.com/j2se/1.3/install-solaris-patches.html for information about any patches that might be needed.</p>
<p>A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up to date.</p>	<p>To use the Japanese online Help, copy the quartus.chm file from the jhhelp directory of the CD-ROM to your /quartus/solaris directory.</p>

HP-UX Only

Issue	Workaround
<p>You receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).</p>	<p>Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: /etc/passwd and /etc/group.</p>
<p>Attempting to convert your device SRAM Object Files (.sof) to Programmer Output Files (.pof) for use with a configuration device, such as an EPC2 device, causes the Quartus II software to “hang” when you open the Conversion Setup File (.cof).</p>	<p>Create the POF as usual and add it to your project with the Add Files to Project command (Project menu).</p>

Issue	Workaround
<p>A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.</p>	<p>To use the Japanese online Help, copy the quartus.chm file from the jhhelp directory of the CD-ROM to your /quartus/hp11 directory.</p>
<p>While programming an EPC16 device with the Quartus II programmer, the software will “hang” and not respond to any inputs.</p>	<p>Program EPC16 devices on Windows NT or Solaris-based computers.</p>
<p>Under some circumstances the Quartus II user interface may “hang” and become unresponsive during compilation on an HP-UX 10.2 workstation. This problem occurs due to a problem in HP-UX 10.2 and does not occur when running on HP-UX 11.0.</p>	<p>Kill the existing <code>quartus</code> process and recompile the project using the command-line. You can then use the UI to view the compilation results.</p>

Linux Only

Issue	Workaround
<p>The MegaWizard Plug-In Manager (Tools menu) may initially appear very small or the Quartus II software may appear to be frozen when you are accessing the Linux version of the Quartus II software using Exceed and the KDE windows manager.</p>	<p>Replace the Java Runtime Environment (JRE) that is installed automatically with the Quartus II software with the JRE version 1.4, which is available at the following URL: http://java.sun.com/j2se/1.4/download.html Run the JRE installation script in a temporary directory to unarchive the JRE version 1.4. Then, make a backup copy of your /quartus/linux/jre1.3.1_02 directory. Next, copy the contents of the temporary directory to your /quartus/linux/jre1.3.1_02 directory, keeping the directory name the same, even though you are using the JRE version 1.4.</p>

Issue	Workaround
<p>A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.</p>	<p>To use the Japanese online Help, copy the quartus.chm file from the jhlp directory of the CD-ROM to your /quartus/linux directory.</p>
<p>If you attempt to exit from the Quartus II software while the Tutorial window is open, the Tutorial window may remain open and may not respond to your commands.</p>	<p>Close the Tutorial window before exiting from the Quartus II software.</p>
<p>If the MasterBlaster™ download cable is not listed in the Available hardware items list in the Hardware Settings tab of the Hardware Setup dialog box, but it is connected properly, you may not have Read/Write permission for the serial (<code>dev/ttySx</code>) port to which the MasterBlaster cable is connected.</p>	<p>Have a system administrator assign Read/Write permission for the appropriate port. This change can be accomplished by adding you to the “uucp” group, or by giving Read/Write permission for the serial port to everyone, using the following command: <code>chmod o+rw /dev/ttySx</code> where <i>x</i> is the serial port affected.</p>
<p>This release of the Quartus II software supports the MasterBlasterMV download cable using either Passive Serial or JTAG modes. Although you can generate Jam Files (.jam) and Jam Byte-Code Files (.jbc), these file types are not supported for device configuration on Red Hat Linux version 7.1. Additionally, the EPC4, EPC8, and EPC16 configuration devices are not supported at this time, and programming times of EPC2 devices may be extremely slow.</p>	<p>For information about using a ByteBlasterMV download cable with the Quartus II software on the Linux operating system, contact Altera Customer Applications.</p>

Issue	Workaround
<p>If you are using the ReflectionX X server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.</p>	<p>Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: <code>setenv QUARTUS_MWWM allwm</code> <code><Enter></code> <code>quartus -no_splash <Enter></code></p>

Device Family Issues

Mercury

Issue	Workaround
<p>If your Quartus II version 1.0 or 1.1 design for a Mercury device uses the <code>altlvds_tx</code> or <code>altlvds_rx</code> megafunction, and you archived the design, you may have functional problems in your design, including inverted signals.</p>	<p>Delete the <code>altlvds_tx</code> or <code>altlvds_rx</code> megafunction from the design and replace it with the version included with the current version of the Quartus II software before compiling your design in the Quartus II software version 2.1 or later.</p>

Excalibur

Issue	Workaround
<p>You may receive the message “System Build Descriptor File missing parameter <code>programming_clock_frequency</code>” for System Build Descriptor Files (<code>.sbd</code>) generated in the Quartus II software version 2.0 and earlier, after selecting the Boot from Serial option in the Excalibur MegaWizard.</p>	<p>Rerun the Excalibur MegaWizard in the current version of the Quartus II software to regenerate the SBD File and correct the error.</p>
<p>You may receive the following error message when simulating the <code>alt_exc_stripe_ess.vhd</code> or <code>ess_hdl.vhd</code> files in the ModelSim software if you have not enabled VHDL93 support: “Attribute foreign has not been declared”</p>	<p>To enable VHDL93 support in the ModelSim software, uncomment the following line in your <code>modlesim.ini</code> file or in your ModelSim project file (<code>.mpf</code>): <code>; VHDL93 = 1</code> Or, you use the <code>vcom -93</code> option when simulating the VHDL files in ModelSim.</p>

Cyclone

Issue	Workaround
If you used the ACEX 2K Support Pack to compile your design in the Quartus II software version 2.1, you must change the specified device family to Cyclone and recompile your design files.	
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
LVDS-compatible pins are not supported in this release.	
The Auto Packed Registers logic option for Cyclone devices has no effect. ⁽¹⁾	To control the Auto Packed Registers option for Cyclone devices, use the Auto Packed Registers -- Advanced logic option. You must set the device family to Stratix to access that option.

(1) This content was added for version 1.1 of these release notes

Stratix

Quartus II Timing Analyzer Reporting Differential I/O Clock f_{MAX} Limits

The Quartus II software version 2.1 including Service Pack 1 incorrectly reports f_{MAX} limits for input and output clocks of Stratix devices for the corresponding I/O standards when differential I/O pins are used.

The actual input and output clock f_{MAX} limits of the Stratix devices are shown in the following tables.

Refer to Table 1 for the actual input clock limits on the specified device pins.

Table 1. Actual Input Clock Limits

Input Clock Limits (MHz)			
I/O Standard	Speed Grade		
	-5	-6	-7
clk[3..0] and clk[11..8] pins			
LVDS	717 (1)	717 (1)	640
LVPECL	717 (1)	717 (1)	640

Input Clock Limits (MHz)			
I/O Standard	Speed Grade		
	-5	-6	-7
HyperTransport	717 (1)	717 (1)	640
3.3-V PCML	400	375	350
Differential HSTL	400	350	300

Table 1. Actual Input Clock Limits (Continued)

Input Clock Limits (MHz)			
I/O Standard	Speed Grade		
	-5	-6	-7
clk[7..4] and clk[15..12] pins			
LVDS	645	645	622
LVPECL	645	645	622
HyperTransport	500	500	450
3.3-V PCML	300	275	275
Differential HSTL	400	350	300
fppllclk[10..7] pins			
LVDS	500	422	311
LVPECL	311	311	311
HyperTransport	350	350	350
3.3-V PCML	275	250	175
Differential HSTL	350	300	250

(1) The Quartus II software limits the input clock to 645 MHz. Contact Altera Applications if you need to achieve up to 717 MHz.

To achieve the highest input clock performance supported by these pins, the signals must be assigned to pins `clk[3..0]` and/or `clk[11..8]`.

Refer to Table 2 for the actual output clock limits on the Fast PLL clocks.

Table 2. Actual Output Clock Limits for Fast PLL clocks

Output Clock Limits (MHz) for Fast PLL Clocks			
I/O Standard	Speed Grade		
	-5	-6	-7
LVDS	645	645	500
LVPECL	645	645	500
HyperTransport	420	420	420
3.3-V PCML	420	420	420

Refer to Table 3 for the actual output clock limits on the Enhanced PLL clock output pins.

Table 3. Actual Output Clock Limits for Enhanced PLL clock output pins

Output Clock Limits (MHz) for Enhanced PLL Clock Output Pins			
I/O Standard	Speed Grade		
	-5	-6	-7
LVDS	500	500	500
LVPECL	500	500	500
HyperTransport	350	350	350
3.3-V PCML	350	350	350

Design Flow Issues

LogicLock

Issue	Workaround
The LogicLock™ regions window may not get refreshed when making a LogicLock assignment such as performing an Import operation.	To see new assignments, you may need to exit from the Quartus II software then restart the Quartus II software.
LogicLock Resources estimation in the Compilation Report is misleading for Stratix devices due to memory or DSP blocks that may be completely or partially within a LogicLock region.	Only logic element resources are reported and are based on the origin of the LogicLock region since the resources available in a rectangular area of a Stratix device depends on the origin of the region.

Verification

Issue	Workaround
Node names for module outputs that are directly connected to inferred objects (counters, etc.) cannot be added to an STP File.	To add such node names to an STP File, you should first assign those names to a signal bus and then add the bus to the STP File.
The data displayed in the SignalTap II waveform display is not correct under some circumstances.	The correct data is captured, but is not displayed unless the STP File is closed and reopened after acquisition. A software patch is available from the Altera Customer Applications department.

Integrated Synthesis (VHDL and Verilog HDL)

Issue	Workaround
<p>The Verilog and VHDL extractors now support the <code>translate_off</code> and <code>translate_on</code> pragmas. Some designs relied on the behavior of the Quartus II software version 2.1 (which ignores pragmas). A common case is where you have a MegaWizard-generated VHDL or Verilog HDL megafunction and have added <code>translate_off</code> and <code>translate_on</code> pragmas to hide the internal details from your 3rd party synthesis tool. The details will also be hidden from the Quartus II software also, and as a result, the megafunctions will not be implemented when you compile using version 2.1 and later of the Quartus II software.</p>	

Issue	Workaround
<p>Some designs that compiled successfully using the Quartus II software version 2.0 may not compile successfully using the Quartus II software versions 2.1 and later. Common issues are:</p> <ul style="list-style-type: none"> • Assigning to a single register in multiple Always Constructs or Process Constructs; the Quartus II software versions 2.1 and later will give a multiply-driven signal error. • Width mismatches in VHDL that were not caught in the Quartus II software version 2.0. • Referring to another generic within a generic list in VHDL, for example having generic WIDTH and generic DATA (WIDTH downto 0). This feature is not officially supported in VHDL, but it is supported in many tools including the Quartus II software version 2.0. It is not supported in the Quartus II software versions 2.1 and later. 	
<p>If you have an IP core in VHDL or Verilog HDL and your license is not set up correctly, you will get a “Can’t open design file” error.</p>	
<p>The Quartus II software versions 2.1 and later connect all nets driven by GND together, and all nets driven by VCC together. This can cause confusing error messages, as an electrical conflict on one GND net may be reported on any GND net, not necessarily the one which is actually causing the problem.</p>	
<p>When you instantiate a non-Verilog HDL module from a Verilog HDL design file, you must use named Parameter Value Assignments to set parameter values.</p>	<p>Altera recommends using a Defparam Statement to set parameter values. Ordered parameters will be ignored when instantiating non-Verilog HDL modules from a Verilog HDL design.</p>

Issue	Workaround
<p>The Quartus II software versions 2.1 and later will give an error when you try to shift or rotate a bit vector by more than the number of bits in the vector. For example, shifting a 32-bit register by 33 bits will cause an error.</p>	<p>You can work around this problem by truncating or taking the modulus of the shift distance as appropriate before doing the shift or rotate.</p>
<p>The Quartus II software assumes that parameters/generics on modules should be inherited. If a parent module has the parameter PARAM and a value of 1 and a child module has a parameter PARAM without an explicit value, the value 1 will be inherited and will override the default value. This behavior is by design and is consistent with previous versions of the Quartus II software, but is not compliant with the VHDL and Verilog HDL language standards.</p>	
<p>The Quartus II software crashes with an Internal Error when a VHDL or Verilog HDL entity instantiates another lower-level entity with a similar name. For example, if a VHDL entity top has a generic integer whose value is 1, and the entity top instantiates a component named top_1, this condition will cause an Internal Error. One example of this crash occurs with the Turbo Encoder/Decoder MegaCore[®] function in decoder mode.</p>	<p>In the case of the Turbo Decoder, the workaround is to instantiate the auktd_umts_turbo_decoder_5_4_4_0 function directly rather than instantiating it via the auktd_umts_turbo_decoder.vhd file. You can inspect the plain-text VHDL file in the /MegaCore/turbo_codec/lib directory to see how this is done. For general user code, change the name of the instantiated entity such that it does not match the <code><top_level_entity_name>_<param1>_<param2>...</code> format.</p>

Verilog HDL Integrated Synthesis

Issue	Workaround
<p>Verilog-2001 mode is enabled by default. This mode can cause some issues with Verilog-1995 designs, most commonly due to new reserved words in Verilog-2001 such as <code>config</code>.</p>	<p>Do not use reserved words as identifiers.</p>

Issue	Workaround
<p>If more than one copy of a module is instantiated, the first instantiation will set the maximum port widths. In other words, if you have</p> <pre>wire [3:0]a; wire [7:0]b;</pre> <pre>mod my_inst_1(a); mod my_inst_2(b);</pre> <p>the port of my_inst_2 will be clipped to 4 bits wide. A warning message is issued.</p>	<p>Move my_inst_2 above my_inst_1.</p>
<p>The Quartus II software versions 2.1 and later do not recognize Verilog HDL state machines. Instead it synthesizes them as generic logic. The Compiler does not report state information and you cannot control the encoding using Quartus II logic options.</p>	<p>A future version of the Quartus II software will recognize Verilog HDL state machines and optimize them to deliver improved performance.</p>
<p>The Quartus II software versions 2.1 and later look for files in an 'include compiler directive in the project root directory. If there is a path specified, it is interpreted as being relative to the project root directory.</p>	
<p>A function call in a vector range specification causes an Internal Error.</p>	
<p>The Quartus II software versions 2.1 and later do not correctly parse a Defparam Statement that contains a space between the module name and the parameter name.</p>	<p>Remove the space between the module name and the parameter name. For example, the following excerpt from a sample design,</p> <pre>foo inst(a,b,c) defparam inst . param = 1;</pre> <p>gives the error “variable name inst is already defined..” If you remove the space between inst and the period, the design compiles correctly.</p>

Issue	Workaround
<p>Wired net types are incorrectly treated as regular nets. The following design should be legal and result in <code>wired_or_net</code> equaling 1</p> <pre>wor wired_or_net; assign wired_or_net=1; assign wired_or_net=0;</pre> <p>However, the Quartus II software versions 2.1 and later treat <code>wired_or_net</code> as a regular wire and issues a warning that the net is driven by multiple drivers. This problem also applies to wired-AND nets.</p>	
<p>Verilog HDL escaped names that look like vectors can cause problems in the Quartus II software. For example, if you have a single-bit component port named <code>\my_vector_port[3:0]</code>, the Quartus II software versions 2.1 and later will treat it as an array port.</p>	<p>You should avoid using escaped port names in the Quartus II software versions 2.1 and later.</p>
<p>In a Case Statement, if you specify a <code>full_case</code> pragma and a default clause, the Quartus II software versions 2.1 and later will ignore the default case. This behavior is different from some other tools which will not ignore the default case.</p>	
<p>The Quartus II software versions 2.1 and later do not allow two parameter value overrides (Defparam Statements) for a parameter. This behavior is different from the IEEE Std. 1364-2001 <i>IEEE Standard Verilog Hardware Description Language</i> manual, in which the last Defparam Statement is used if there are multiple Defparam Statements.</p>	

Issue	Workaround
<p>The Quartus II software versions 2.1 and later do not give an error for a Defparam Statement for a parameter that does not exist in the named module, or for a Parameter Value Assignment with more unnamed parameters than are defined in the module.</p>	
<p>If you use the following statement: <pre>// synthesis Translate_off</pre> followed by <pre>/* synthesis translate_on */</pre> you will get a syntax error.</p>	<p>Replace <pre>/* synthesis translate_on */</pre> with <pre>//synthesis translate_on.</pre></p>
<p>If the last line of your Verilog Design File (.v) is a 'define compiler directive and there is no carriage return at the end of the line, the Quartus II software versions 2.1 and later give a syntax error.</p>	<p>Add a carriage return at the end of the line to avoid receiving the syntax error message.</p>
<p>Recursive Verilog HDL functions or modules, such as a module that instantiates itself, cause the Compiler in the Quartus II software versions 2.1 and later to crash.</p>	

Issue	Workaround
<p>The Verilog HDL reader in the Quartus II software versions 2.1 and later do not differentiate internally between bit vectors and strings. This is compliant with the IEEE Std. 1364-2001 <i>IEEE Standard Verilog Hardware Description Language</i> manual, but can cause problems in mixed-language designs, such as commonly occur when instantiating MegaCore functions. When evaluating parameters from a Verilog HDL module, the Quartus II software versions 2.1 and later will write a bit vector as a string if its size is a multiple of 8 bits and if each 8-bit value represents a valid ASCII character. For example, the value:</p> <pre>defparam inst.p = 16'h4849;</pre> <p>will be passed to module <code>inst</code> as the string "HI".</p> <p>This problem occurs with the PCI Compiler MegaCore function when a Verilog HDL wrapper is generated using the MegaWizard Plug-In Manager (Tools menu).</p>	<p>If you are instantiating the PCI Compiler MegaCore function, you should regenerate the core wrapper and choose to output an AHDL or VHDL version to use in your project instead of the Verilog HDL version. If the bit vector is less than 32 bits wide, you can replace it with an integer, which is not subject to the same problem. For the example, you would replace the value <code>16'h4849</code> with the integer equivalent:</p> <pre>defparam inst.p = 18505;</pre>

VHDL Integrated Synthesis

Issue	Workaround
The Quartus II software versions 2.1 and later do not synthesize <code>a < b</code> for user-defined enums.	
<p>The Quartus II software versions 2.1 and later do not support ranges in Case Statements on an enum. For example:</p> <pre> type state_type is (st_a, st_b, st_c, st_d, st_e); case cur_st is ... when st_b to st_d => next_st <= st_e; ... </pre>	

EDA Integration Issues

Issue	Workaround
The 220model.vhd simulation library, located in the <code>\<Quartus II directory>\eda\sim_lib</code> directory, contains VHDL 87-compliant models.	For a VHDL 93-compliant simulation model library, you can download an updated version of this simulation model library from the Altera web site, at http://www.altera.com .
This version of the Quartus II software does not support the Amplify Physical Optimization software, even though you can select it in the EDA Tool Settings dialog box.	Do not select the Amplify Physical Synthesis Optimization software in the EDA Tool Settings dialog box.
The directory containing the ARM-based Excalibur stripe models changed in the Quartus II software version 2.0. This change may cause compilation scripts that were created for earlier versions of the Quartus II software to fail.	Edit your compilation scripts so that the models and simulation wrapper files are located in the following directory: quartus\eda\sim_lib\excalibur\stripe_model_<operating system>\ModelGen\models\epxa<1 / 4 / 10>\r0\<simulator_language>

Software Issues Resolved

This Quartus II software Service Pack corrects issues in the following areas:

- Corrected problems with Verilog Output File (**.vo**) when generating a Power Input File (**.pwf**).
- Made substantial improvements to support for I/O standards on Stratix family devices.
- Fixed an internal error with product-term technology mapping in MAX 7000 devices.
- Improved support for clock data synchronization (CDS) in APEX II devices.
- Corrected a problem in which Excalibur device PLL settings were incorrect under certain circumstances.
- Updated Excalibur device PLL support to correspond to final device specifications after characterization.
- Fixed issues in native synthesis of VHDL and Verilog HDL files.
- Fixed internal errors in the Fitter that occurred when RAM was used in Stratix devices and some RAM inputs were left unconnected.
- Made substantial improvements to behavioral simulation models for Stratix devices.
- Fixed an internal error in the Fitter that occurred when certain netlist optimization settings were used in conjunction with SignalProbe signals.
- Fixed a fitting issue that occurred with PLLs in Stratix devices.
- Fixed an internal error in the Fitter that occurred for Stratix device PLLs.
- Corrected VO File problems with virtual pins.
- Corrected problems with power estimation when running the Quartus II software on Linux workstations.
- Fixed an internal error that occurred in the Timing Analyzer in conjunction with SignalProbe signals.
- Fixed an internal error that occurred when saving STP Files.
- Corrected a display refresh error in the SignalTap II Logic Analyzer.
- Fixed an internal error in the Block and Symbol Editor when adding a symbol to a schematic.
- Fixed an internal error in the Assembler that occurred in conjunction with the `alt_ddio` megafunctions for designs targeted for Stratix devices.
- Fixed an issue with Excalibur Slave Binary Image Files (**.sbi**) that limited the accessible address space.
- Fixed an internal error in the Compiler that occurred when compiling designs that contain PLL targeted for ACEX 1K devices.
- Corrected an error in timing analysis for some registered carry chains in Stratix and Mercury devices.
- Corrected errors in the Pin-Out Files (**.pin**) for Stratix devices, which had the incorrect voltage for some VCC pins.
- Corrected an error in the VHDL Output File (**.vho**) for designs targeted to ACEX 1K devices.

- Fixed an issue in the Database Builder that occurred with case-sensitive names.
- Fixed incorrect compilation results of designs targeted to Stratix devices in conjunction with the `INIT_DONE` pin option.
- Corrected problems in support for all SSTL-type differential I/O standards in Stratix devices.
- Fixed an internal error that occurred when compiling designs containing PLLs target APEX 20KE devices.
- Corrected problems with open-drain pin equations in designs targeted to APEX II devices.
- Fixed an internal error that occurred when using the MasterBlaster download cable on Linux workstations.
- Fixed a problem that occurred when using the **Logic Cell Insertion** option in designs targeted to ACEX 1K devices.

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