



Quartus II Software Release Notes

April 2003

Quartus II version 2.2 Service Pack 2

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **quartus** directory.

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New Features & Enhancements

The Quartus II software version 2.2 Service Pack 2 includes the following changes:

- Adds advanced compilation and simulation support for the new Cyclone™ EP1C4 devices in 324-pin and 400-pin FineLine BGA® packages
- Adds full programming support for Cyclone EPC1C3, EP1C6, and EP1C12 devices
- Adds full programming support for Stratix™ EP1S10, EP1S20, EP1S40, EP1S60, and EP1S80 devices
- Adds support for the new USB-Blaster™ download cable
- Provides final timing models for Stratix EP1S10, EP1S20, EP1S25, EP1S30, and EP1S40 devices
- Provides enhancements to licensing functions
- Adds a “speed vs. area” trade-off option for the `dcfifo` megafunction
- Many software enhancements

Device Support & Pin-Out Status

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Stratix	EP1S10ES F484	EP1S10 F484
	EP1S10 F672	EP1S10 B672
	EP1S10 F780	EP1S20 F484
	EP1S20 F484	EP1S40 F780
	EP1S60 B956	EP1S60 F1020
	EP1S60 F1508	EP1S80 F1020
Cyclone	EP1C3 T100	EP1C3 T144
	EP1C6 F256	EP1C12 Q240
	EP1C12 F256	EP1C12 F324

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Cyclone	EP1C4 F324	EP1C4 F400

Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Devices with Initial Information Support

Device Family	Devices
None	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	Notes
Stratix	EP1S60	The Quartus II software version 2.2 includes preliminary timing models for -5, -6, and -7 speed grades for the Stratix device family.
	EP1S80	
Stratix GX	EP1SGX10	
	EP1SGX25	
	EP1SGX40	
Cyclone	EP1C3	
	EP1C6	
	EP1C12	
	EP1C20	

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
APEX™ II	EP2A15	2.1
	EP2A25	2.1
	EP2A40	2.1
	EP2A70	2.1
APEX™ 20KC	EP20K200C	2.0 SP1
	EP20K400C	2.0
	EP20K600C	2.0
	EP20K1000C	2.0 SP1
Excalibur™	EPXA1	2.0 SP2
	EPXA4	2.0 SP2
	EPXA10	2.0 SP1
Mercury™	EP1M350	2.0
	EP1M120	2.1 SP1
MAX™ 7000	EPM7032AE	2.0
	EPM7064AE	2.0
	EPM7128AE	2.0
	EPM7256AE	2.0
	EPM7512AE	2.0
	EPM7032B	2.0
	EPM7064B	2.0
	EPM7128B	2.0
	EPM7256B	2.0
	EPM7512B	2.1 SP1
MAX 3000	EPM3032A	2.0
	EPM3064A	2.0
	EPM3128A	2.0
	EPM3256A	2.0
	EPM3512A	2.1 SP1
Stratix	EP1S10	2.2 SP2
	EP1S20	2.2 SP2
	EP1S25	2.2 SP2
	EP1S30	2.2 SP2
	EP1S40	2.2 SP2

The current version of the Quartus II software also includes final timing models for the ACEX[®] 1K, APEX 20KE, FLEX[®] 6000, and the FLEX 10KE device families. Final timing models for these device families became final in versions earlier than version 2.0.

EDA Interface Information

The Quartus II software version 2.2 Service Pack 2 supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink [®] support
Mentor Graphics [®] LeonardoSpectrum [™] -Altera	2002f	✓
Mentor Graphics [®] LeonardoSpectrum [™]	2002f	✓
Synopsys Design Compiler	2002.02	
Synopsys FPGA Compiler II	3.7	✓
Synplicity Synplify and Synplify Pro	7.2	✓
Aplus Design Technologies (ADT) PALACE [™]	2.3	✓
Verification Tools	Version	NativeLink support
Cadence NC-Verilog	3.4 (s013)	✓
Cadence NC-VHDL	3.4 (s013)	✓
Cadence Verilog-XL	3.3	
Model Technology [™] ModelSim [®]	5.6a	✓
Model Technology ModelSim-Altera	5.6a	✓
Innoveda BLAST	1.2.2	
Synopsys PrimeTime	2000.05	✓
Synopsys Scirocco	2000.12	✓
Synopsys VSS	2000.05	
Synopsys VCS	6.0.1	
Mentor Graphics Tau	2.2	
Verplex Conformal LEC	3.4.0.a	

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
<p>The Quartus II software no longer uses the registry to store non-user interface-related settings. Non-user interface-related settings are stored automatically in the quartusii.ini file when you open the Quartus II software user interface for the first time.</p>	<p>You must open the Quartus II software user interface at least once before using the command-line version of the software.</p>
<p>Versions of the Quartus II software earlier than version 2.0 cannot open Block Design Files (.bdf) created with the Quartus II software version 2.0 and later.</p>	
<p>Not all speed grades of a given device share the same features.</p>	<p>Refer to the Altera data sheet for the device family for further information.</p>
<p>The default setting for the Power-Up Don't Care logic option has been changed to On in the Quartus II software version 2.1 Service Pack 1 and later.</p>	
<p>There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.</p>	<p>Connect the port to a top-level bidirectional pin or to other logic in the design.</p>
<p>To use the EP20K400GC655 device in your design, please contact the Altera Customer Applications Department.</p>	
<p>If you have a version of the Quartus[®] software earlier than the Quartus II software version 1.0 installed on your computer in addition to the Quartus II software, you can start the previous version of the program only by running the runq.exe program from the \quartus\bin directory that contains the earlier version you wish to use.</p>	

Issue	Workaround
<p>You should not create multiple Compiler settings that have the same design entity as the “compilation focus.”</p>	
<p>Under some circumstances, if the Optimize I/O cell register placement for timing option in the Fitting page of the Settings dialog box (Assignments menu) is turned on and you are using multiple peripheral clock enable signals, you may receive an error message or the Quartus II software may crash.</p>	<p>Set the Clock Enable Routing logic option to Single-Pin for some of the clock enable signals.</p>
<p>Context-sensitive Help is not available for some items in the Quartus II software.</p>	<p>To locate Help on those items, choose Index (Help menu) and type the name of the item.</p>
<p>For APEX 20KE devices, the Quartus II software provides limited support for the following I/O standards that are not available with the I/O Standard logic option:</p> <ul style="list-style-type: none"> • LVPECL is a differential I/O standard that is similar to the LVDS I/O standard. APEX 20KE devices can support LVPECL I/O pins by using the I/O pins in LVDS mode with an external resistor network. • PCI-X is an enhanced version of the PCI I/O standard that can support a higher average bandwidth. This standard has more stringent requirements than PCI. 	<p>To use the LVPECL I/O standard in APEX 20KE devices in the Quartus II software, set the I/O Standard logic option for the pins to LVDS and connect the pins to an appropriate external resistor network.</p> <p>The APEX 20KE I/O drivers meet the requirements for PCI-X. Turn on the PCI I/O logic option to support PCI-X requirements, including the overshoot clamp.</p>
<p>You cannot locate the source of an error in a design file if compilation was unsuccessful due to a syntax error.</p>	
<p>If you open a project that was created using an earlier version of the Quartus II software, you may receive a message that indicates that the database is incompatible and that results of the last compilation will be lost.</p>	<p>To maintain existing placement information, back-annotate all of the project assignments in the earlier version. Then, delete the <code>\<project name>\db</code> directory and all of its contents.</p>
<p>The Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.</p>	<p>Make clock settings assignments to all non-PLL clocks.</p>

Issue	Workaround
If you are using the <code>lpm_mult</code> megafunction, you must turn off the Auto Cascade Chains option when editing project defaults in the Default Logic Options page of the Settings dialog box (Assignments menu).	
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the Group command (Edit menu) to create groups of arbitrary nodes.
Using the Cancel button in the Assignment Organizer (Assignments menu) when multiple nodes have been selected causes the Quartus II software to restore the setting(s) of the first node to all the nodes that were edited.	Do not use the Cancel button to cancel changes made to two or more selected nodes that have assignments of differing settings.
If you are using the <code>altcam</code> , <code>altclklock</code> , <code>altlvds_rx</code> , or <code>altlvds_tx</code> megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Last Compilation floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name file.eda.edif .	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (<code>debug[7..0]</code>), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying “Unsupported data type in the top-level module.”	Reserve the pins using single name notation (for example, <code>debug7</code> , <code>debug6</code> , and so on).
The Quartus II software versions 2.1 and later supports only version 5.2 and later of the Altera PowerKit™ software. Previous versions of the PowerKit software are not supported with these versions of the Quartus II software.	

Issue	Workaround
If you are using the HSTL Class II I/O standard with an APEX II device, additional information is required.	Contact the Altera Customer Applications department at apexii@altera.com for information about Service Packs and device pin-outs.
Do not change the file permissions (such as changing “read-only” to “read and write”) of Quartus II settings and configurations files (.csf, .esf, and so on) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
The order of ports for the ARM[®]-based Excalibur MegaWizard[®] Plug In -generated symbol for the stripe changed in version 2.0 of the Quartus II software. If you re-run the MegaWizard Plug-In Manager (Tools menu) for a design created in a version of the Quartus II software earlier than version 2.0, you will receive port connection errors when you compile the design.	To avoid receiving these errors, adjust the port connections in the BDF after updating the symbol.
Node names containing numbers greater than 2 ³¹ -1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
The Quartus II software versions 2.1 and later no longer support the Compiler Settings File (.csf) <code>MIGRATION_DEVICES</code> variable.	In order to specify migration device names in the CSF, use the <code>DEVICE_MIGRATION_LIST</code> variable. For example: <code>DEVICE_MIGRATION_LIST = "DEVICE_A,DEVICE_B,DEVICE_C" ;</code>
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the CSF or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the Assignment Organizer (Assignments menu) or by manually editing the CSF.	If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.
You may receive an “invalid command name” error when you run an existing Tcl script that uses the Tk toolkit for its user interface. Beginning with the Quartus II software version 2.2, the Quartus II software no longer initializes the Tk toolkit automatically when starting any process.	Add the Tcl command “init_tk” to the beginning of any Tcl script that uses Tk.

Issue	Workaround
<p>The lpm_fifo MegaWizard Plug-In has been removed from the Quartus II software version 2.2. The <code>lpm_fifo</code> megafunction is still included for backward compatibility with older designs.</p>	<p>Altera recommends that you use the lpm_fifo+ MegaWizard Plug-In for all new designs requiring single-clock FIFO functions.</p>
<p>If you receive an error message saying “System resources low...” or if the user interface is slow in responding and there is a lot of disk activity when you are not compiling a design, your system may be running out of free memory.</p>	<p>You can recover system memory by clearing messages from the Messages window. To clear messages from the Messages window, right-click anywhere in the Messages window and choose Clear Messages from Window (right button pop-up menu). Additional memory can be recovered by closing the Floorplan Editor.</p>
<p>Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.</p>	<p>Delete the Quartus Workspace File (.qws) <code><project name>.qws</code> from the project directory. If the problem persists, delete the <code><project directory>\db</code> directory.</p>
<p>When you are setting phase shift and duty cycle values for clock signals using the <code>altpll</code> megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.</p>	<p>You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.</p>
<p>If you are using the Quartus II Web Edition software version 2.2, the software may crash if you compile a design while the Current Assignments floorplan is open.</p>	<p>Close the Current Assignments floorplan before compiling the design.</p>
<p>A synchronization problem with the <code>altshift_taps</code> megafunction that caused a problem when the read and write address counters were assigned to different LABs has been fixed.</p>	<p>If your design uses the <code>altshift_taps</code> megafunction, you should recompile the design with the Quartus II software version 2.2 Service Pack 2.</p>

Platform-Specific Issues

PC Only

Issue	Workaround
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the stdole32.tlb file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p>Windows 98: <CD-ROM drive letter>:\win98\extract.exe /A /L %SystemRoot%\System base4.cab stdole32.tlb <Enter></p> <p>Windows 98SE: <CD-ROM drive letter>:\extract.exe /A /L %SystemRoot%\System base4.cab stdole32.tlb <Enter></p> <p>Windows NT: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows 2000: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows XP: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p>
<p>It is possible that one of the Quartus II executable files (quartus.exe, quartus_cmd.exe, quartus_swb.exe, quartus_dbc.exe, quartus_sim.exe, or quartus_cmp.exe) may not terminate properly after an error.</p>	<p>Use the Windows Task Manager to end the process before running the Quartus II software again.</p>

Issue	Workaround
<p>If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.</p>	<p>Limit the full, hierarchical instance name to fewer than 247 characters if possible.</p>
<p>If you are running the Quartus II software under the Windows 2000 operating system using a node-locked (single-user) license that is locked to a network interface card number (NIC ID), and are not physically connected to the network, the Quartus II software will not be able to determine your NIC ID and will not allow you to compile a design. This problem also occurs if you are running a FLEXlm license server under the Windows 2000 operating system with a license locked to the NIC ID.</p>	<p>Follow the recommendations given on the following Microsoft Knowledge Base web page: http://support.microsoft.com/support/kb/articles/Q239/9/24.asp</p>
<p>The Quartus II software will not operate if your computer has multiple active network interface cards (NICs).</p>	<p>If you have more than one NIC, you must deactivate all but one in order to run the Quartus II software.</p>
<p>A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.</p>	<p>To use the Japanese online Help, copy the quartus.chm file from the jhlp directory of the CD-ROM to your \quartus\bin directory.</p>
<p>If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the \quartus\bin directory.</p>	<p>You must share the quartus directory, not the \quartus\bin directory.</p>
<p>If you are running the ZoneAlarm personal firewall software, you may receive a message saying, "Can't start or continue to run database creator" when you launch the Quartus II software.</p>	<p>The Quartus II software is not compatible with the ZoneAlarm software. The ZoneAlarm software mistakenly determines that the Quartus II software is accessing the Internet when it uses TCP/IP for its inter-process communication. You must disable the ZoneAlarm software to run the Quartus II software.</p>

Issue	Workaround
The Quartus II software installation program does not add the path for the Quartus II software to the PATH statement in your autoexec.bat file when installed under Windows 98.	Add the path for your installed Quartus II software to the PATH statement in your autoexec.bat file manually.
Under some circumstances, the Quartus II software crashes when using the “X” button to close the Print Preview window if a project is open.	Use the Close button to close the Print Preview window if you have a project open.
If you disconnect your network connection while the Quartus II software is open, you may receive an error message saying “Can't start or continue to run the db creator.”	Close the Quartus II software before disconnecting the network connection and wait for the “LAN is disconnected” message in the Windows Taskbar before restarting the Quartus II software.
The Quartus II software is not compatible with the MATLAB web server.	Turn off the MATLAB web server in the Services Control Panel (Windows Start menu) before running the Quartus II software.
Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear.	The registry settings controlling the position of the Quartus II windows may have become corrupted. Type the following command at a command prompt: <code>quartus -reset_desktop <Enter></code>
Path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters.
Under some circumstances, the Quartus II software may run correctly the first time it is started after installation, then fail to run with a “License Not Found” error thereafter.	If you have specified multiple license servers in either your LM_LICENSE_FILE environment variable or on the License Setup page of the Options dialog box (Tools menu), you must make the license server that serves the Quartus II software license the first server specified on the line.
On computers running the Windows 98 or Windows 98SE operating system, downloading device data at speeds less than 57,600 baud can result in failed downloads.	Download device data at speeds of 57,600 baud or greater when operating under Windows 98 or Windows 98SE.
The installation method for the driver for the ByteBlaster, ByteBlasterMV, and ByteBlaster II download cables has changed. The instructions in the <i>Quartus II Installation & Licensing Manual for PCs</i> are incorrect.	Use the bblpt.exe utility to install or remove the necessary driver. The utility program is automatically installed in the same directory as the pgdhdlc.sys device driver file. If you need to install the driver, change to the driver directory, and type <code>bblpt /i <Enter></code> at a command prompt.

Solaris, HP-UX & Linux

Issue	Workaround
<p>The Quartus II Help is not available if you have set either the MWNO_RIT or the MWDONT_XINITTHREAD environment variables before running the Quartus II software.</p>	<p>Remove the variables from your environment and allow the Quartus II software to set these variables automatically, if needed.</p>
<p>If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.</p>	<p>Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.</p>
<p>Under some circumstances, there may be editor windows listed in the Window menu that you cannot see.</p>	<p>To display the hidden windows, choose Cascade (Window menu).</p>
<p>You cannot launch the AXD Debugger software from within the Quartus II software.</p>	<p>Launch the AXD Debugger software from outside the Quartus II software.</p>
<p>If you use the License Setup page of the Options dialog box (Tools menu) to enter the location of the license file, the Quartus II software may give an “Unable to Find License” message.</p>	<p>Restart the Quartus II software before compiling your design.</p>
<p>Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.</p>	<p>Specify the full path to your web browser software on the Internet Connectivity page of the Options dialog box (Tools menu). If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.</p>
<p>The Colors list in the Block & Symbol Editor Color Options page of the Options dialog box (Tools menu) or Format tab of the Properties dialog box (Edit menu) for any object in the Block or Symbol Editors may remain open, and may cause an internal error if you click anywhere else in the Quartus II software before closing the Colors list box.</p>	<p>Select a color to close the Color list box.</p>
<p>You cannot run the Innoveda BLAST software automatically from within the Quartus II software, even if the Run this tool automatically after compilation option is turned on.</p>	<p>Run the Innoveda BLAST software manually outside the Quartus II software.</p>

Issue	Workaround
You cannot run the Mentor Graphics LeonardoSpectrum software from within the Quartus II software even if the Run this tool automatically after compilation option is turned on.	Run the LeonardoSpectrum software manually outside the Quartus II software.
You cannot run the Model Technology ModelSim software from the EDA Tool Post-Compilations Options > Run Simulation Tool command (Processing menu) from within the Quartus II software.	Run the ModelSim software outside the Quartus II software.
You can access the Quartus II online Help by typing <code>hh quartus.chm</code> <Return> at a command prompt.	
If you attempt to exit from the Quartus II software while the Tutorial window is open, the Tutorial window may remain open and may not respond to your commands.	Close the Tutorial window before exiting from the Quartus II software.
When the LogicLock Regions window is floating, you cannot drag and drop node names to it from the Node Finder.	Dock the LogicLock Regions window before dragging node names to it from the Node Finder.

Solaris Only

Issue	Workaround
The ARM-based Excalibur MegaWizard Plug-In , which is available from the MegaWizard Plug-In Manager requires the Java Runtime Environment (JRE) version 1.3, which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for JRE 1.3 to function properly.	Check the web site http://java.sun.com/j2se/1.3/install-solaris-patches.html for information about any patches that might be needed.
A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.	To use the Japanese online Help, copy the quartus.chm file from the jhelp directory of the CD-ROM to your /quartus/solaris directory.

Issue	Workaround
If you attempt to exit from the Quartus II software while the Tutorial window is open, the Tutorial window may remain open and may not respond to your commands.	Close the Tutorial window before exiting from the Quartus II software.

HP-UX Only

Issue	Workaround
You receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).	Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: /etc/passwd and /etc/group .
Attempting to convert your device SRAM Object Files (.sof) to Programmer Output Files (.pof) for use with a configuration device, such as an EPC2 device, causes the Quartus II software to “hang” when you open the Conversion Setup File (.cof).	Create the POF as usual and add it to your project with the Add Files to Project command (Project menu).
A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.	To use the Japanese online Help, copy the quartus.chm file from the jhlp directory of the CD-ROM to your /quartus/hp11 directory.
When programming an EPC16 configuration device with a MasterBlaster download cable at 115,200 bps, the Quartus II software crashes.	Use 38,400 bps or slower when programming on HP-UX workstations.

Linux Only

Issue	Workaround
The MegaWizard Plug-In Manager (Tools menu) may initially appear very small or the Quartus II software may appear to be frozen when you are accessing the Linux version of the Quartus II software using Exceed and the KDE windows manager.	Replace the Java Runtime Environment (JRE) that is installed automatically with the Quartus II software with the JRE version 1.4, which is available at the following URL: http://java.sun.com/j2se/1.4/download.html Run the JRE installation script in a temporary directory to unarchive the JRE version 1.4. Then, make a backup copy of your /quartus/linux/jre1.3.1_02 directory. Next,

Issue	Workaround
	copy the contents of the temporary directory to your /quartus/linux/jre1.3.1_02 directory, keeping the directory name the same, even though you are using the JRE version 1.4.
A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.	To use the Japanese online Help, copy the quartus.chm file from the jhhelp directory of the CD-ROM to your /quartus/linux directory.
If the MasterBlaster™ download cable is not listed in the Available hardware items list in the Hardware Settings tab of the Hardware Setup dialog box, but it is connected properly, you may not have read/write permission for the serial (<code>dev/ttySx</code>) port to which the MasterBlaster cable is connected.	Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the “uucp” group, or by giving read/write permission for the serial port to everyone, using the following command: <code>chmod o+rw /dev/ttySx</code> where <i>x</i> is the serial port affected.
This release of the Quartus II software supports the ByteBlasterMV download cable using either Passive Serial or JTAG modes. Although you can generate Jam Files (.jam) and Jam Byte-Code Files (.jbc), these file types are not supported for device configuration on Red Hat Linux version 7.1. Additionally, the EPC4, EPC8, and EPC16 configuration devices are not supported at this time, and programming times of EPC2 devices may be extremely slow.	For information about using a ByteBlasterMV download cable with the Quartus II software on the Linux operating system, refer to the <i>Quartus II Installation & Licensing Manual for UNIX and Linux Workstations</i> , or contact Altera Customer Applications.
If you are using the ReflectionX X server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.	Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: <code>setenv QUARTUS_MWWM allwm <Enter></code> <code>quartus -no_splash <Enter></code>
The Quartus II software may crash if you enter a value outside the acceptable range in the Guideline spacing box in the Block/Symbol Editor General Options page or in the Width controls in the Waveform Editor Printing Options page or in the	Enter only values that are available in the list.

Issue	Workaround
<p>Default file size controls in the Memory Editor General Options page of the Options dialog box (Tools menu).</p>	
<p>The Compilation Report for the Quartus software version 2.2 displays a different Build Number (146) than does the About dialog box (Help menu) which displays Build Number 147.</p>	<p>The Build Number shown in the Compilation Report is correct because the Compiler was not changed in Build 147.</p>

Device Family Issues

Mercury

Issue	Workaround
<p>If your Quartus II version 1.0 or 1.1 design for a Mercury device uses the <code>altlvds_tx</code> or <code>altlvds_rx</code> megafunction, and you archived the design, you may have functional problems in your design, including inverted signals.</p>	<p>Delete the <code>altlvds_tx</code> or <code>altlvds_rx</code> megafunction from the design and replace it with the version included with the current version of the Quartus II software before compiling your design in the Quartus II software version 2.1 or later.</p>

Excalibur

Issue	Workaround
<p>You may receive the message “System Build Descriptor File missing parameter <code>programming_clock_frequency</code>” for System Build Descriptor Files (.sbd) generated in the Quartus II software version 2.0 and earlier, after selecting the Boot from Serial option in the ARM-based Excalibur MegaWizard Plug-In.</p>	<p>Rerun the ARM-based Excalibur MegaWizard Plug-In in the current version of the Quartus II software to regenerate the SBD File and correct the error.</p>
<p>You may receive the following error message when using the Excalibur Stripe Simulator (ESS) in the ModelSim software if you have not enabled VHDL93 support: “Attribute foreign has not been declared”</p>	<p>To enable VHDL93 support in the ModelSim software, uncomment the following line in your modelsim.ini file or in your ModelSim project file (.mpf): <code>; VHDL93 = 1</code> Or, you can use the <code>vcom -93</code> option when simulating the VHDL files in the ModelSim software.</p>

Issue	Workaround
<p>If you are using the Stripe-to-PLD Bridge in Excalibur EPXA10 Devices, your design may not function due to the Stripe-to-PLD Bridge lockup errata if either of the following options is turned on in the Quartus II software:</p> <p>Remove Redundant Logic Cells Perform WYSIWYG Primitive Resynthesis</p> <p>Please refer to the EPXA10 Device Errata Sheet for details on the device errata.</p>	<p>To avoid bridge lock-up, ensure that the Remove Redundant Logic Cells option is turned off for the project.</p> <p>If the Perform WYSIWYG Primitive Resynthesis option is turned on for your project, you may receive warnings that the stripe signals were not routed correctly. To eliminate the warnings, re-run the MegaWizard Plug-In Manager in the Quartus II version 2.2 software. This procedure will create an additional settings file (alt_exc_stripe.esf) to ensure that the required logic elements are implemented.</p>
<p>The SOPC Builder CD GNU Tools installer does not include the <i><GnuPro tools for ARM path>\bin</i> directory in the system path. As a result, if you run a makefile to build your software, you will receive one of the following errors:</p> <p>“arm-elf-ld: cannot open <i><path to SOPC Builder>/bin/arm-gnupro/arm9-020528//lib/gcc-lib/arm-elf/2.96-arm9-020528/crtbegin.o</i>: No such file or directory”</p> <p>or</p> <p>“Unable to Locate DLL: The dynamic link library cygwin1.dll could not be found in the specified path <i><system path></i>”</p>	<p>Perform the following steps:</p> <ol style="list-style-type: none"> 1. Manually add the path to the GnuPro tools for ARM, for example: <i><sopc install dir>\bin\arm-gnupro\arm9-020528\bin</i>, to the beginning of your system path environment variable. 2. Copy the cygwin1.dll from <i><SOPC Builder install dir>\cygwin\bin</i> to <i><SOPC Builder install dir>\bin\arm-gnupro\arm9-020528\bin</i> <p>or</p> <p>Run the GnuPro tools for ARM from within the Quartus II software version 2.2 instead of using a makefile.</p>

Cyclone, Stratix & Stratix GX

Issue	Workaround
<p>For Stratix, Stratix GX, and Cyclone device families, the Quartus II software version 2.2 introduces the Minimize Area With Chains setting for the Auto Packed Registers option. When you compile a design with that setting, and then back-annotate the fit but demote logic cell locations to LABs, the subsequent compilation may result in a no-fit.</p>	<p>Perform one of the following workarounds:</p> <ul style="list-style-type: none"> • If you used the Minimize Area With Chains setting, do not demote cell assignments to LABs. <p><i>or</i></p> <ul style="list-style-type: none"> • Save the post-fitting netlist from the first compilation as a Verilog Quartus Mapping File (.vqm) for use in subsequent compilations. This option allows you to demote assignments to LABs.
<p>In some cases, using the Minimize Area With Chains setting for the Auto Packed Registers option can cause a no-fit due to the way a particular carry chain is packed with registers that have location constraints. You might receive one of the following messages:</p> <p>“Error: Can't place carry chain that starts with node <node name>”</p> <p><i>or</i></p> <p>“Info: One or more nodes in carry chain have location assignments”</p> <p>The usual symptom is that the carry chain is longer than one LAB, but the first and last nodes will be constrained to the same row (Y-coordinate).</p>	<p>Set the Auto Packed Registers option to OFF for all nodes in the carry chain that cannot be placed.</p>
<p>If you assign I/O pins to the same I/O Bank as pins used by the <code>alt_ddio_out</code> or <code>alt_ddio_bidir</code> megafunctions, the Quartus II software may issue a “no fit” error even though your design may not use those pins simultaneously. The Quartus II compiler automatically restricts the proximity of high data-rate pins to permit simultaneous switching of those pins.</p>	<p>Contact Altera Applications for additional information if necessary.</p>

Issue	Workaround
<p>If you have an LE that is the first LE in a subtraction carry chain, and you constrain this particular LE to a location that is not the first LE in the lab (i.e., not LE 0), then the Quartus II software may crash with an internal error. This is due to the fact that the first LE in a subtraction chain needs to be in location 0 in the LAB.</p>	<p>Change the LE-specific constraint to a more general LAB constraint or eliminate the constraint all together.</p>
<p>The <code>dcfifo</code> megafunction has been improved to decrease the logic cell usage. A new <code>ADD_RAM_OUTPUT_REGISTER</code> parameter has been added. When the parameter is set to OFF, the logic cell usage is decreased, but f_{MAX} may also decrease. When the parameter is set to ON, logic cell usage will increase, but f_{MAX} will be improved. The default setting is OFF.</p>	<p>If your design uses the <code>dcfifo</code> megafunction, and you wish to decrease the logic cell usage, add the <code>ADD_RAM_OUTPUT_REGISTER</code> parameter and set it to ON. You must recompile your design after this change.</p>

Stratix

Issue	Workaround
<p>Versions of the Quartus II software earlier than version 2.2 did not correctly implement the following functions in DSP blocks in Stratix devices:</p> <ul style="list-style-type: none"> • Mixed sign multiplications of 19 bits and greater • Dynamic sign multiplications of 19 bits and greater • Signed multiplications greater than 36 bits 	<p>Designs that implement DSP functions must be recompiled in the Quartus II software version 2.2 or later. The Quartus II software version 2.2 will implement the design correctly, but will use more resources and have reduced performance from earlier versions.</p>
<p>Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.</p>	

Changes to Stratix PLL Timing:

Enhanced PLL Maximum Clock Frequency (MHz)			
Speed Grade	-5	-6	-7
Quartus II Ver. 2.2	1000	1000	1000
Stratix Datasheet Ver. 3.0	800	800	800
Quartus II Ver. 2.2 SP1	800	800	600

Fast PLL Maximum Clock Frequency (MHz)			
Speed Grade	-5	-6	-7
Quartus II Ver. 2.2	1000	1000	1000
Stratix Datasheet Ver. 3.0	840	840	840
Quartus II Ver. 2.2 SP1	1000	1000	700

For Enhanced PLLs (EPLLs):

The Quartus II software version 2.2 SP1 and later will enforce the 300–800 MHz clock frequency range as specified in the Stratix device family data sheet for -5 and -6 speed grades. The clock frequency range for the -7 speed grade is 300–600 MHz.

For Fast PLLs (FPLLs):

The Quartus II software version 2.2 SP1 and later will continue to support the 300–1000 MHz clock frequency range when the FPLL is used as a general purpose PLL. The higher clock frequency range enables more flexibility in choosing multiplication and division factors in the Quartus II software. When the FPLL is used in Source Synchronous mode, the clock frequency range is unchanged from the data sheet specification of 300–840 MHz.

Stratix GX

The Stratix GX device family supports the following I/O standards on the RX data input pins. However, the Quartus II software version 2.2 and later supports only 1.5-V PCML on the RX data inputs in AC-coupled mode. If you wish to use the LVDS or LVPECL I/O standards with AC coupling, you must assign the pins to the **1.5-V PCML** I/O standard in the Quartus II software.

	RX data inputs	
	AC-coupled	DC-coupled
1.5-V PCML	✓	✓
LVDS	*	
LVPECL	*	
3.3-V PCML		

* will be supported in version 3.0

Issue	Workaround
<p>When you are using the MegaWizard Plug-In Manager (Tools menu) to generate a symbol for an <code>altgxb</code> megafunction for a protocol that is neither GigE or XAUI, you should enable the <code>rx_clkout</code> port (receiver output clock) in the MegaWizard Plug-In, unless it is being used in transmitter-only mode or if you are performing parallel loopback.</p> <p>The data signals (<code>rx_out</code>, <code>rx_patterndetect</code>, <code>rx_syncstatus</code>, <code>rx_ctrlldetect</code>, <code>rx_disperr</code>, <code>rx_errdetect</code>, <code>rx_ala2sizeout</code>) from the receiver will then be synchronized to the <code>rx_clkout</code> clock signal.</p>	
<p>Currently the simulation models provided for the <code>altgxb</code> megafunction do not model the power-up condition correctly for simulation in other EDA simulation tools.</p>	<p>You must manually set the <code>pll_areset</code> signal to power up high in your test bench or simulation vector file. Refer to “Perform a Functional Simulation...” topics in the “Using Other EDA Simulation Tools” section of the Quartus II Help for more information.</p>

Issue	Workaround
When using the dedicated GXB clock pins to drive altgxb megafunction ports inclk and rx_crucclk, the Compilation Report will indicate that the negative pin does not have a 100/120/150 Ohm on-chip termination (OCT) setting (assuming that the positive pin has a 100/120/150 Ohm OCT setting).	No action is required, this problem is a reporting issue only and the programming file is correct and will correctly enable the OCT setting.

Cyclone

Issue	Workaround
If you used the ACEX 2K Support Pack to compile your design in the Quartus II software version 2.1, you must change the specified device family to the Cyclone device family and recompile your design files.	
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
The Cyclone EP1C3 T100 device does not support the LVDS I/O standard on any pins.	Use the Cyclone EP1C3 T144 device instead. It supports the LVDS I/O standard.

APEX 20K, APEX 20KC, APEX 20KE & APEX II

Issue	Workaround
Regardless of the settings made in the Critical Path Settings dialog box (View menu), the Floorplan Editor will not display critical paths that have memory as their source or destination.	Use the Timing Analyzer to determine critical paths that begin or end in memory.

APEX II

Issue	Workaround
If you use the altddio_in or altddio_bidir megafunction and do not connect the dataout_h and dataout_l ports, you will receive an error message and the design will fail to compile.	Connect the dataout_h and dataout_l ports.

Design Flow Issues

Verification

Issue	Workaround
Node names for module outputs that are directly connected to inferred objects (counters, and so forth) cannot be added to a SignalTap II File (.stp).	To add such node names to an STP File, you should first assign those names to a signal bus and then add the bus to the STP File.
Projects containing an STP File that contains nodes specified for incremental routing may display the captured data incorrectly if the specified nodes fail to route. In that case, you might receive a “Can’t route SignalTap II incremental connection” message. Instead of displaying the data for the node named in the message as Unknown (X), the data will be displayed as either High (1) or Low (0).	
If you select SignalTap II: pre-synthesis or SignalTap II: post-fitting in the Filter list of the Node Finder and select a bus to add to the STP File, the Quartus II software may expand the bus into individual nodes that may be removed during synthesis, resulting in an error.	Delete the nodes and recompile the project. You can select individual nodes in the Node Finder and group them in the SignalTap II window using the Group command (Edit menu).
If you select SignalProbe in the Filter list of the Node Finder, buses and groups of nodes may not be displayed.	Use the Design Entry filter setting instead.
The pre-compiled simulation libraries for NC-Verilog and NC-VHDL must be compiled on the platform (PC, Solaris, or HP) on which you intend to use the libraries. Only the simulation libraries for Windows are provided with the Quartus II software.	Contact the Altera Applications department for pre-compiled simulation libraries for NC-Verilog or NC-VHDL on Solaris or HP-UX.

Simulation

Issue	Workaround
<p>The PLLs in designs targeted to Stratix devices sometimes do not simulate correctly in other EDA simulation tools. The PLLs do not lock when you are driving the <code>altlvds_tx</code> megafunction with the <code>altlvds_rx</code> clock, or if you are driving the <code>altlvds_rx</code> megafunction with the <code>altlvds_tx</code> clock.</p>	<p>Make the following changes to the VHDL or Verilog HDL files generated by the MegaWizard Plug-In Manager and the <code>altlvds_tx</code> or <code>altlvds_rx</code> megafunctions.</p> <p>When using the <code>altlvds_tx</code> clock output to drive the <code>altlvds_rx</code> PLL, make the following changes:</p> <p>For VHDL :</p> <pre> COMPONENT altlvds_rx GENERIC (clk_src_is_pll : STRING and altlvds_rx_component : altlvds_rx GENERIC MAP (clk_src_is_pll > "on" </pre> <p>For Verilog HDL:</p> <pre> altlvds_rx_component.clk_src_is _pll = "on"; </pre> <p>Or when using the <code>altlvds_rx</code> clock output to drive the <code>altlvds_tx</code> PLL, make the following changes:</p> <p>For VHDL :</p> <pre> COMPONENT altlvds_tx GENERIC (clk_src_is_pll : STRING and altlvds_tx_component : altlvds_tx GENERIC MAP (clk_src_is_pll > "on" </pre> <p>For Verilog HDL:</p> <pre> altlvds_tx_component.clk_src_is _pll = "on"; </pre>

Integrated Synthesis (VHDL and Verilog HDL)

Issue	Workaround
<p>The Verilog and VHDL extractors now support the <code>translate_off</code> and <code>translate_on</code> pragmas. This change in support may cause problems in some designs that relied on the behavior of the Quartus II software versions earlier than version 2.1, which ignore pragmas. A common case is where you have a MegaWizard-generated VHDL or Verilog HDL megafunction and have added <code>translate_off</code> and <code>translate_on</code> pragmas to hide the internal details from your EDA synthesis tool. If you use those pragmas, the details will also be hidden from the Quartus II software, and as a result, the megafunctions will not be implemented when you compile using the Quartus II software version 2.1 and later.</p>	
<p>Some designs that compiled successfully using the Quartus II software version 2.0 may not compile successfully using the Quartus II software version 2.1 and later. Common issues are:</p> <ul style="list-style-type: none"> • Assigning to a single register in multiple Always Constructs or Process Constructs. The Quartus II software version 2.1 and later will give a multiply-driven signal error. • Width mismatches in VHDL that were not caught in the Quartus II software version 2.0 and earlier. • Referring to another generic within a generic list in VHDL, for example having generic WIDTH and generic DATA(WIDTH downto 0). This feature is not officially supported in VHDL, but it is supported in many tools including the Quartus II software version 2.0. It is not supported in the Quartus II software version 2.1 and later. 	

Issue	Workaround
If you have an IP core in VHDL or Verilog HDL and your license is not set up correctly, you will get a “Can’t open design file” error.	Refer to <i>Application Note 205: Understanding Altera Licensing</i> and <i>Application Note 229: Advanced Troubleshooting for Altera Licensing</i> for more information on setting up your license.
The Quartus II software version 2.1 and later connect all nets driven by GND together, and all nets driven by VCC together. This can cause confusing error messages, as an electrical conflict on one GND net may be reported on any GND net, not necessarily the one that is actually causing the problem.	
When you instantiate a non-Verilog HDL module from a Verilog HDL design file, you must use named Parameter Value Assignments to set parameter values.	Altera recommends using a Defparam Statement to set parameter values. Ordered parameters will be ignored when instantiating non-Verilog HDL modules from a Verilog HDL design.
The Quartus II software versions 2.1 and later will give an error when you try to shift or rotate a bit vector by more than the number of bits in the vector. For example, shifting a 32-bit register by 33 bits will cause an error.	You can work around this problem by truncating or taking the modulus of the shift distance as appropriate before doing the shift or rotate.

Verilog HDL Integrated Synthesis

Issue	Workaround
Verilog-2001 mode is enabled by default. This mode can cause some issues with Verilog-1995 designs, most commonly due to new reserved words in Verilog-2001 such as <code>config</code> .	Do not use Verilog-2001 reserved words as identifiers or select Verilog-1995 on the Verilog HDL input page under HDL Input Settings of the Settings dialog box (Assignments menu).
The Quartus II software version 2.1 and later does not recognize Verilog HDL state machines. Instead it synthesizes them as generic logic. The Compiler does not report state information and you cannot control the encoding using Quartus II logic options.	A future version of the Quartus II software will recognize Verilog HDL state machines and optimize them to deliver improved performance.

Issue	Workaround
<p>The Quartus II software version 2.1 and later looks for files in an 'include compiler directive in the project root directory and the user library directories. If there is a path specified, it is interpreted as being relative to the project root directory or the user library directory.</p>	
<p>A function call in a vector range specification causes an Internal Error.</p>	
<p>Verilog HDL escaped names that look like vectors can cause problems in the Quartus II software. For example, if you have a single-bit component port named <code>\my_vector_port[3:0]</code>, the Quartus II software versions 2.1 and later will treat it as an array port.</p>	<p>You should avoid using escaped port names in the Quartus II software version 2.1 and later.</p>
<p>The Quartus II software version 2.1 and later does not allow two parameter value overrides (Defparam Statements) for a parameter. This behavior is different from the IEEE Std. 1364-2001 <i>IEEE Standard Verilog Hardware Description Language</i> manual, in which the last Defparam Statement is used if there are multiple Defparam Statements.</p>	
<p>The Quartus II software version 2.2 and later issues a warning message when it encounters a Defparam Statement for a parameter that does not exist in the instantiated module, but it will compile successfully. Future versions of the software will issue an error message and will NOT compile successfully.</p>	<p>Remove the unnecessary parameter so the design will compile successfully in future versions of the Quartus II software.</p>
<p>Recursive Verilog HDL functions or modules, such as a module that instantiates itself, cause the Compiler in the Quartus II software version 2.1 and later to crash.</p>	

EDA Integration Issues

Issue	Workaround
<p>The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for ATOPS mode, which is currently not supported by the Amplify software.</p>	<p>Contact Synplicity for the support schedule for the Amplify software ATOPS mode.</p>
<p>The directory containing the ARM-based Excalibur stripe models changed in the Quartus II software version 2.0. This change may cause compilation scripts that were created for earlier versions of the Quartus II software to fail.</p>	<p>Edit your compilation scripts so that the models and simulation wrapper files are located in the following directory: <code>\quartus\eda\sim_lib\ excalibur\ stripe_model_<operating system> \ModelGen\models\epxa<1 / 4 / 10>\r0\<simulator_language></code></p>
<p>There is not an option in the installation program to install the EDA tool interface for the Cadence Concept software, even though the software is supported by the Quartus II software version 2.2.</p>	<p>Select Cadence Verilog-XL in the installation to install the cadence.tcl interface script in your <code><Quartus II installation>/eda/cadence</code> directory.</p>
<p>When generating test bench files from waveform files in the Waveform Editor, if you add a single signal from a bus to the waveform file, the Quartus II software will create a signal in the test bench file with the entire bus notation as the name of the signal, instead of as a single bit on a bus.</p>	<p>Create a group in the waveform file and assign the explicit bit from the bus to the group before generating the test bench file.</p>
<p>The Cadence NC-VHDL version 3.4 software requires the s013 patch, which contains a more stable version of the NC-VHDL software.</p>	<p>Install the s013 patch, available from Cadence, for the NC-VHDL software before simulating designs.</p>

Software Issues Resolved

This Quartus II software Service Pack corrects issues in the following areas:

- Added support for USB-Blaster on PCs
- Added support for a grace period after License expiration
- Added support for Raw Programming Data Files (**.rpd**) for Active Serial Configuration devices
- Added an option to the `dcfifo` megafunction to allow the user to choose between higher speed or smaller area
- Updated Timing Models for Stratix, Stratix GX, and Cyclone devices to reflect updated silicon characterization data

- Changed Stratix GX transceiver pre-emphasis settings display
- LVDS I/O transmitter and receiver support for a deserialization factor of 7 in Stratix devices
- Stratix DQS simulation models
- `dcfifo` megafunction simulation models
- Stratix DSP block simulation models
- APEX II RAM simulation models
- Stratix RAM simulation models
- Stratix I/O simulation models
- Internal errors in the Fitter and Assembler for designs targeting Cyclone devices
- Internal error in the Fitter when using the SignalProbe feature
- Internal error in the Netlist Writer
- Internal errors in the Assembler for designs targeting Stratix and Stratix GX devices
- Error in the Altera JTAG Server system service software
- Errors in the generation of Standard Delay Format Output Files (`.sdo`)
- Incorrect compilation results for designs that use Dual-Port RAM and target Stratix devices
- Long compilation times when using assignments containing wildcard characters
- Errors that caused unused M4K memory blocks in Stratix devices to consume too much power
- Errors in the Fitter for designs targeting Stratix GX devices
- Errors in the `altgxb` megafunction
- Error in the Assembler for designs targeting Cyclone devices that have VREF pins assigned
- Error in the `lpm_mult` megafunction
- Error in the Assembler for designs targeting Stratix devices that use the On-Chip Termination feature
- Error in the Compilation Report generation in which some timing requirements were not reported
- Incorrect processing of state machines
- Error in the inference of shift registers during synthesis

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