

Engineering Change Order (ECO) Support in Programmable Logic Design

A major benefit of programmable logic is that it accommodates changes to the system specification late in the design cycle. In a typical engineering project system development cycle, the specification for the programmable logic portion is likely to change when engineering development begins or when all system elements are being integrated.

These last-minute design changes are commonly referred to as engineering change orders (ECOs). ECOs are defined as small changes to the functionality of a design, after the design has been fully compiled, i.e., synthesis and place-and-route are completed.

ECOs are usually intended for errors found in the programmable logic design during debug or changes that are made to the programmable logic design specification to compensate for design problems in other areas of the system design, the operation of which cannot easily be changed in these areas.

As the project nears completion, a significant amount of time and effort has been invested in achieving timing closure in the programmable logic device (PLD). It is crucial that the programmable logic design flow is optimized to support ECOs in an efficient manner.

Impact of Last Minute Design Changes

ECOs have an impact on many areas of a system design, including:

- Performance
- Compile time
- Verification
- Documentation

Performance

When a small change is made to the design functionality, it can result in previous design optimizations being lost. Typical examples of design optimizations are floorplan optimizations and physical synthesis. Ideally, there should be a means to preserve the design optimizations that have already been made. This will focus future optimizations that may have to be made to the design to the areas of the design to which the ECO changes were made.

Compile Time

In the traditional programmable logic design flow, a small change in the design results in a complete recompilation of the design, i.e., synthesis and place-and-route. Thus, the process of making small changes to the design in order to reach the final implementation on a board can be a very long process. Ideally, in order to reach the desired functionality and to reach timing closure, a small change in functionality should result in a reduced compilation time. This can be achieved using incremental compilation technology that uses the previous fit information on the areas of the design that have not been affected by the ECOs.

Verification

After a small design change, the impact of the change on the design needs to be verified. This is typically achieved through timing analysis and simulation. The designer requires the ability to perform a complete verification on the design. The designer may choose to limit the verification to the area of the design that is impacted by the ECOs. Thus, the designer must be able to run timing analysis on select paths and have the option to perform simulation on gate level and timing simulation netlists.

Documentation

Changes to the project files must be tracked. This helps other users reproduce the results at a later date. Ideally, users should be able to have multiple compilation revisions, so that they can try out changes without corrupting the results that they have previously obtained.

ECO Support

ECOs can be applied at either of two different stages of a typical design flow:

- HDL level
- Netlist level

Traditionally in programmable logic design, ECOs have been applied at the HDL level. This is generally because the tools to easily create ECOs and to enable design sign-off at the netlist level have not been available for PLDs.

ECO Support at the HDL Level

An ECO at the HDL level is a small incremental change to the design's Verilog or VHDL source. This change may range from a single line to several lines of code modified within a module or entity. Typical examples of such modifications are:

- Changes to the state encoding of a finite state machine
- Addition of pipeline register(s) to improve design performance
- Signal duplication to reduce fan-out

- Adding a term to a conditional expression
- Changing the polarity of register control signals

A few changes to the source code can produce many changes to the netlist produced by 3rd party EDA synthesis or the Quartus® II software's integrated synthesis. During the synthesis process, the synthesis tools generally preserve the names of registers from the HDL source code, but automatically generate names for the combinational (look-up table level) nodes. This automatic name generation is necessary to accommodate the synthesis optimization performed on the HDL source in order to use the target device resources more efficiently.

Thus, a minor source code change can result in a many changes to the names used in the synthesis netlist. The changes in the synthesis netlist can be due to either:

- The node names in the new netlist implement different functionality than in the previous netlist
- The node names in the new netlist implement mainly the same functionality as in the previous netlist, but have different names

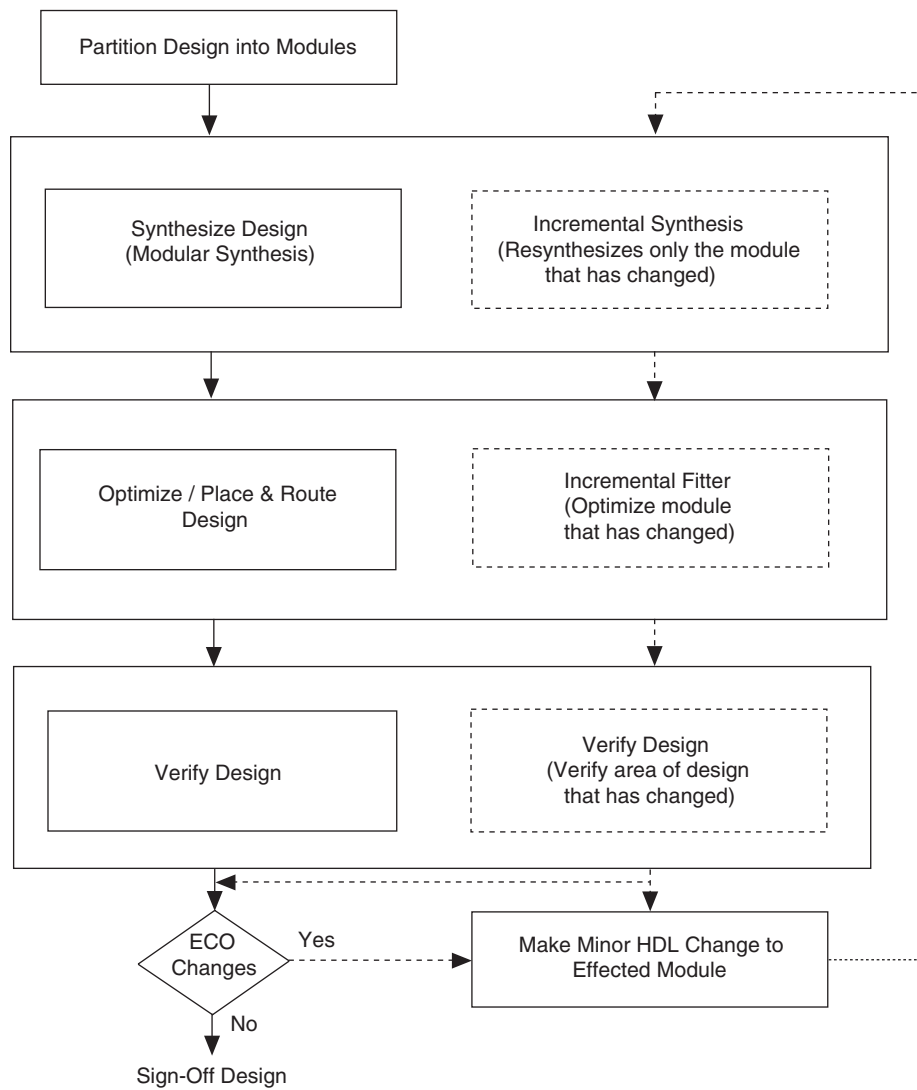
In order to leverage the previous design optimizations and to reduce the compilation time, there must be a means of performing an incremental compilation on the nodes with the new functionality and preserving the previous optimizations on the nodes that have not changed. Thus a means of identifying nodes that maintain the same functionality but have different names is essential for providing an ECO flow that truly works. Such a solution is provided with the incremental fitting option available in the Quartus II software version 3.0.

The Quartus II incremental fitting feature performs a netlist comparison between the original synthesis netlist and the new netlist containing the ECO changes. It matches nodes based upon names, functionality, fan-in, and fan-out. Those nodes that can be matched inherit the assignments from the previous fit.

Thus, the incremental fitting feature can preserve existing fitting information and timing. This limits any timing and fitting changes to the logic that has changed in functionality and reduces the compilation time using the incremental fitting capability.

In order to limit the changes caused by ECOs, it is recommended that users adopt a modular design flow. A modular design flow combined with the incremental compilation features mentioned previously minimizes the changes in performance caused by ECOs and also reduces compilation time. Partitioning the design to adopt a modular design flow facilitates the placing of each module in the floorplan for performance. The Quartus II software provides the LogicLock™ feature to optimize the floorplan of modular designs. Altera AN 161: Using the LogicLock Methodology in the Quartus II Design Software describes how to apply LogicLock to a modular design flow. Figure 1 details the recommended design flow to support ECO changes at the HDL level.

Figure 1. Design Flow to Support ECO Changes



ECO Support at the Netlist Level

For certain ECO changes, it can be quicker to make changes at the netlist level rather than at the HDL level. This is the case when the designer is debugging the design on silicon and needs a very fast turnaround in generating a programming file for debugging in system.

A typical application is that the designer uncovers a problem on the board and is able to isolate the problem to the appropriate nodes or I/O cells on the PLD. The designer needs to be able to quickly correct the functionality of the offending logic cell or the properties of the I/O cell and generate a new programming file in minutes. By doing this, the

designer can verify the operation of the change without having to modify the HDL and performing a synthesis and place-and-route operation. This minimizes the disruption to the board verification procedure.

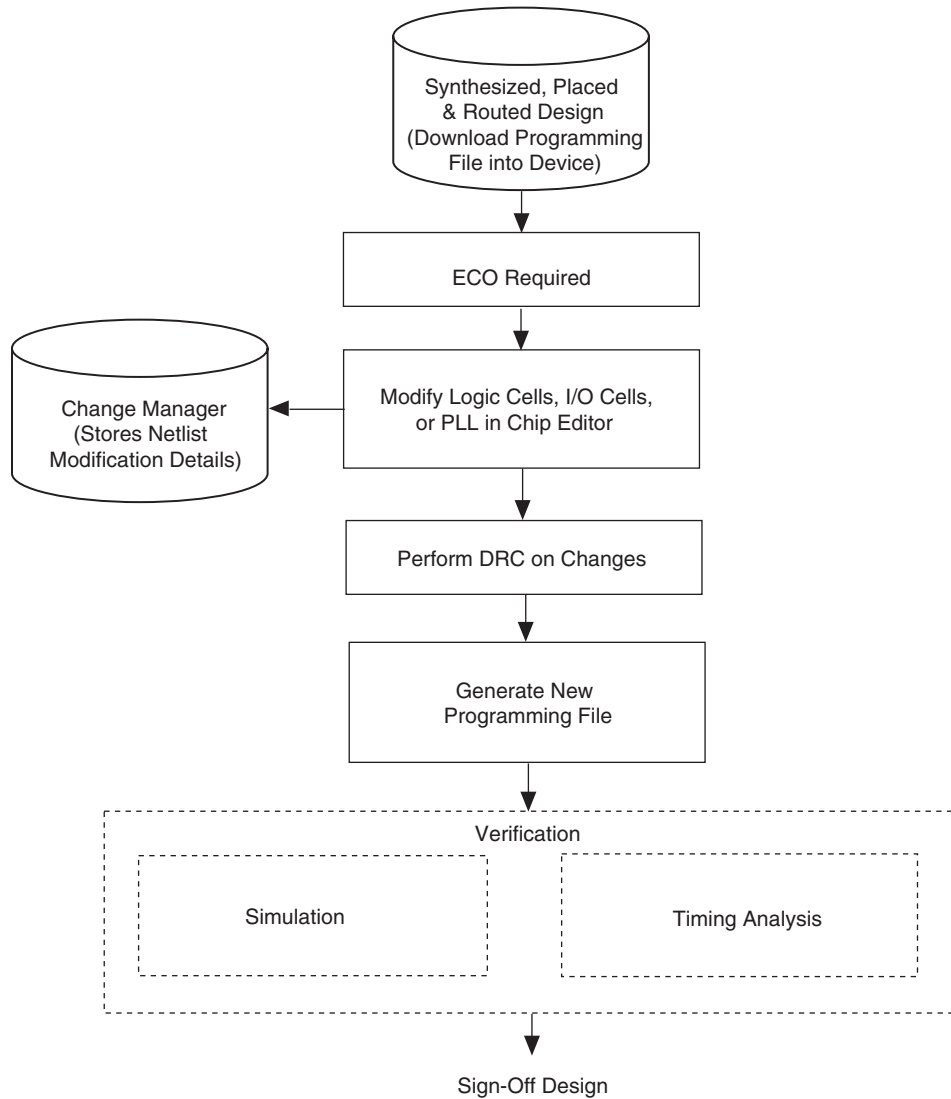
If this quick fix works, the user need not necessarily change the HDL source code and rerun place-and-route. The user should have the option to:

- Document the change that has been made
- Easily recreate the steps taken to produce the changes to the design
- Generate EDA simulation netlists for verification of the design
- Perform timing analysis on the design

These capabilities are provided in the chip editor feature of the Quartus II software.

The Quartus II Chip Editor allows users to make functional changes to individual logic cells and to the I/O cell and phase-locked loop (PLL) parameters. These changes are stored in the Quartus II change manager log. This allows designers to control the application of the changes and more importantly to generate a tool command language (Tcl) file containing the Tcl commands to enable the designer to recreate the changes on the original netlist. This effectively documents the changes made to the project and enables designers to recreate the changes on the original design files at a later date without having to change the HDL source. The designer can regenerate an EDA simulation netlist for the modified design, if it is necessary to perform a gate-level simulation of the modified design. If the designer needs to rerun timing analysis to sign-off the design, timing analysis can be rerun on the netlist containing the ECO changes. Figure 2 details the flow for ECO changes at the netlist level.

Figure 2. Design Flow for ECO Changes at the Netlist Level



Conclusion

Support for ECOs requires a combination of a modular design methodology and the appropriate software design tools.

The Quartus II software version 3.0 provides designers with the software tools and the design methodology to successfully perform ECOs at both the HDL and netlist level for programmable logic designs. This enables designers to reduce the design cycle time and to reach timing closure faster on designs that require last minute design changes.



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