

Delivering RISC Processors in an FPGA for \$2.00

The introduction of the Cyclone™ FPGA family provides system designers with a new platform for creating user-definable microprocessor-based systems. This document illustrates the range of possibilities for integrated systems using Nios® embedded processors, soft intellectual property (IP) cores, and Cyclone devices.

The Nios embedded processor is a configurable 32-bit RISC processor. Nios embedded systems can be created with any number of peripherals. Table 1 shows the base core sizes for the Nios embedded processor. Table 2 lists some of the IP core peripherals that integrate with the Nios embedded processor to form complete micro processing units (MPUs). Most peripherals listed can be parameterized to fit the specific application and can be instantiated multiple times within a single MPU. In addition, customer-designed logic and peripherals can be integrated with the Nios processor to deliver a unique MPU. The creation of these custom MPUs can be done in minutes using the Altera® SOPC Builder tool, and synthesized to run on any Altera FPGA. In addition to the IP cores listed in Table 2, SOPC Builder features additional IP cores available from Altera and our Altera Megafunction Partners Program (AMPPSM) partners.

Table 1. Base Nios Embedded Core Sizes

| Nios Embedded Processor | Logic Element (LE) Count | Embedded RAM |
|-------------------------|--------------------------|--------------|
| 16-bit data path | 950 | 2 blocks |
| 32-bit data path | 1,250 | 3 blocks |

Table 2. Common Peripherals Supplied with the Nios Processor

| Peripheral | LE Count |
|--|----------|
| UART, fixed baud rate | 170 |
| Timer | 244 |
| serial peripheral interface (SPI): 8-bit master, 1 slave | 103 |
| SPI: 8-bit master, 2 slaves | 108 |
| SPI: slave, 8-bit | 98 |
| SPI: slave, 16-bit | 127 |
| General-purpose I/O: 8-bit, tri-state | 45 |
| General-purpose I/O: 16-bit, tri-state | 81 |
| General-purpose I/O: 32-bit, tri-state | 138 |
| General-purpose I/O: 32-bit, input only | 16 |
| General-purpose I/O: 32-bit, output only | 24 |
| SDRAM controller | 380 |
| External memory/peripheral: 32-bit | 110 |
| External memory/peripheral: 16-bit | 85 |

Designers can create practical systems that occupy approximately one-half of the smallest Cyclone device. Table 3 represents the elements of a complete system capable of interfacing with a variety of external devices. The design runs from internal memory and is fully contained in the Cyclone device. This system could be used to control an A/D converter or similar SPI device while receiving control information over a serial interface or Ethernet.

Table 3. Nios System with UART, SPI, Ethernet MAC Interface

| Component | LE Count |
|---|----------|
| Nios central processing unit (CPU): 32-bit data path | 1,250 |
| UART | 156 |
| SPI | 116 |
| External Ethernet media access controller (MAC) interface | 75 |
| RAM (4K) | 25 |
| Avalon™ bus | 115 |
| Total | 1,737 |

Table 4 represents the elements of a complete system using the narrow data-path option of the Nios processor. In this design, the Nios processor would be able to interface to an external content-addressable memory (CAM) controller, respond to the push-button panels, illuminate status LEDs, and communicate to a host system over a high-speed serial link.

Table 4. Nios System with UART, SPI, 16 General-Purpose I/O Pins

| Component | LE Count |
|---|----------|
| Nios CPU: 16-bit data path | 950 |
| UART | 156 |
| SPI | 116 |
| General-purpose I/O: 8-bit, input only | 4 |
| General-purpose I/O: 8-bit, output only | 6 |
| RAM (2K) | 24 |
| Avalon bus | 58 |
| Total | 1,314 |

Table 5 lists the elements of the standard Nios 32-bit reference design shipped with the Nios development board. This design provides a large addressable memory range to address off-chip SRAM and flash memory. Each general-purpose I/O component is parameterized to the exact needs of the interface. The on-chip ROM stores a monitor program that allows the user to download software applications to run out of the external SRAM. On the Nios development board implementation, the flash memory stores a factory-supplied FPGA as well as a user-definable image.

Table 5. Nios 32-bit Reference Design Elements (Note 1)

| Component | LE Count |
|---|----------|
| 32-bit Nios CPU | 1,879 |
| UART | 169 |
| General-purpose I/O: LCD port | 43 |
| General-purpose I/O: LED Port | 8 |
| General-purpose I/O: 7-Segment LED Port | 8 |
| General-purpose I/O: Push-Button Port | 101 |
| Timer (32-bit) | 228 |
| 32-bit SRAM interface | 110 |
| 16-bit flash memory (1 Mbyte addressable) | 110 |
| On-chip ROM with boot monitor | 25 |
| Avalon bus | 289 |
| Total | 2,952 |

Note to Table 5:

- (1) The f_{MAX} for this design is >100 MHz.

Conclusion

With the wide range of densities available in Cyclone devices and the small sizes of Nios embedded systems, system designers can divide complex problems into smaller tasks and use multiple Nios embedded processors. These Nios processors can be customized with a wide-selection of peripherals, defining very simple to very complex MPU systems. By targeting Cyclone devices, powerful, customized embedded systems can be realized at the best cost in the industry.



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